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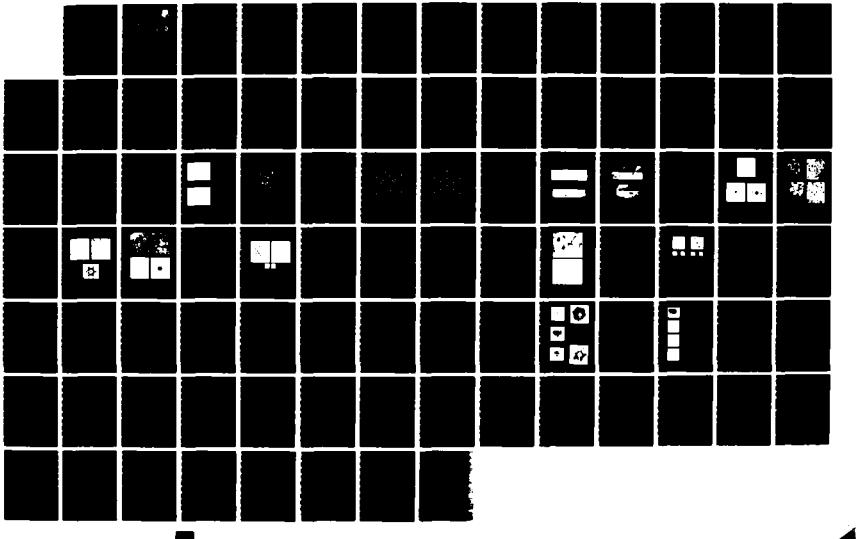

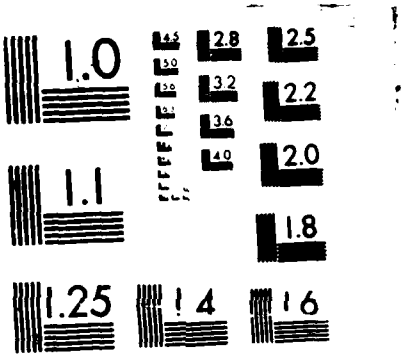

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Final Technical Report
October 1986

ENHANCED INTERNAL PHOTOEMISSION STUDY

Westinghouse Electric Corporation

Richard McKee, Leroy Colquitt, James Greggi and Michael Janocko

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

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19 ABSTRACT (Continue on reverse if necessary and identify by block number)

Both theoretical modeling and physical and electrical characterization of PtSi Schottky gate infrared sensors are reported. ~~Initially,~~ a photoemission model for infrared photoresponse of thin film PtSi Schottky devices has been developed including diffuse photoelectron scattering at the metal/semiconductor interface, film thickness, grain size and defect density effects. For film thickness/effective electron and phonon mean free path (d/L*) ratios >.2, the photoyield is degraded by a rough metal/semiconductor interface, decreasing to a factor of 1/2 for d/L* = 1.

Cross sectional and planar TEM work on ~80A PtSi revealed epitaxial growth of PtSi (with three variants), smoother metal/semiconductor interface, slightly larger grains (200A to 500A) and a more interconnected grain structure for PtSi formed (111) Si as opposed to (100) Si. PtSi films on both substrate orientations are continuous and have thickness variations <15% of the film thickness. TEM work on 20A PtSi on (111) Si still shows good

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coverage epitaxial films with the PtSi pseudohexagonal cell being partially constrained to fit the hexagonal Si cell. These films were formed in vacuum with an anneal of 400°C to 650°C.

Ir response measurements revealed no improvement upon changing the substrate orientation from (100) Si to (111) Si for PtSi films of similar thicknesses. The best C values were obtained on films formed on the (111) Si with values of 19%/eV and a barrier value of 0.225 eV and a barrier value of 0.225 eV for 10A PtSi films. 80A PtSi films formed on both substrate orientations showed curvature on Folwer plots near the barrier value. When the film thickness decreases, this curvature disappeared and was accompanied by shifts in the extrapolated optical barrier as much as .1eV. Leakage on the best diodes exhibited values of 10^{-6} amps/cm^2 at 77K at 3 volts reverse bias with soft breakdown. Since cross-sectional TEM measurements show rougher surfaces for 80A PtSi films on (100) Si as opposed to (111) Si, the lack of change in response implies a D/L* ratio <.2 from our modeling analysis.

17. COSATI CODES (Continued)

Field	Group
20	02

about

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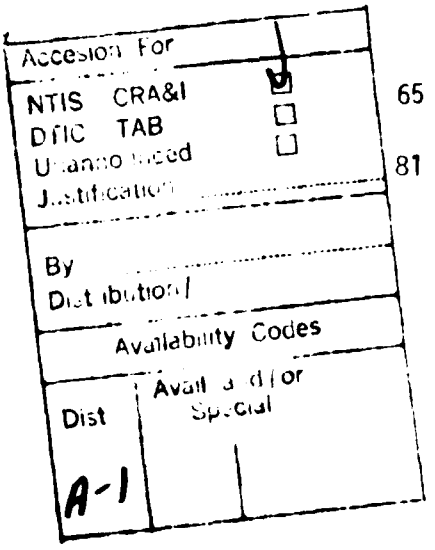


I. OBJECTIVE

Conduct a research program designed to determine the optimum metallurgy for fabricating PtSi/p-Si Schottky diodes for infrared detection in order to improve their performance in accordance with Section J, Attachment No. 2, "Statement of Work," dated November 23, 1983 and provide data in accordance with Contract Date Requirement List (Section J, Attachment No. 1, DD Form 1423, dated May 13, 1983).

II. OVERVIEW OF PROGRESS

A. Technical Progress

The final goal of this research program is to determine the optimum metallurgy for fabricating PtSi/p-Si Schottky diodes for infrared detection in order to improve their quantum efficiency by a factor of 2 over the state of the art PtSi/p-Si Schottky diodes. From the work on this contract, it has been determined that even though PtSi forms epitaxialy on (111) Si and not on (100) Si, our studies show that there is no IR response enhancement of the diodes in using (111) Si over (100) Si.

This study began with a model of the internal photoemission process, which uses parameters including the degree of epitaxy, grain size and defect density. In parallel with this modeling, experimental work was begun. This experimental work included preliminary process development work on fabricating PtSi films on blank (111) Si and (100) Si wafers along with RED and resistivity analysis. Concurrently, PtSi/p-Si diodes were fabricated using a redesigned mask set. Finally, crystallographic analysis and infrared photoresponse work was performed on PtSi layers fabricated on (111) and (100) Si. The following paragraphs highlight the main accomplishments.

1. Photoemission Model

This theoretical work is intended to guide our experimental program centered on improving device performance by realizing good epitaxial PtSi films and to establish a framework for subsequent analysis. In this study, we concentrated on relating the critical parameters of the theory of photoemission to experimentally measured parameters which characterize the silicide, such as the degree of epitaxy, grain size, and defect density.

Our results show that diffuse scattering at the metal/semiconductor interface has a significant influence on the photoyield, with the degree of influence depending on the ratio of the film thickness to the hot electron mean free path, d/L^* . At low temperatures, L^* is dominated by bulk defect scattering. It is difficult, however, to make independent measurements of L^* and estimates are arrived at only indirectly. Estimates of L^* are found in the literature ranging from 60 to several hundred angstroms.

Our results show that for $d/L^* > 0.2$, the photoyield of a device with a perfectly rough interface is degraded when compared to the results for a device with a smooth interface: the difference increases with increasing d/L^* and rises to a maximium of a factor of two for $d/L^* = 1$. For $d/L^* < 0.2$, the photoyield for a rough surface is greater than that produced by a device with a smooth interface.

The hot-electron mean free path is a critical parameter not only of this theory but of conventional photoyield theory as well; special attention paid to theoretical and experimental means of obtaining independent estimates of L^* would improve device design capabilities.

If one interprets the gains in device performance observed by Mckee on expitaxial Pd_2Si as due to improved interface quality, one would expect that d/L^* is > 0.2 and that the best photoyield for PtSi may be obtained through techniques designed to optimize the film epitaxy.

The results of our analysis also show that, for grain boundaries normal to the metal boundaries, grain boundary scattering has no effect on the photoyield. This is a consequence of the special specular scattering properties of grain boundaries. This result confirms experimental evidence which shows the photoyield to be weakly dependent on the size of grains.

Subsequently, we identified two key issues which we believed to have promise for our PtSi optimization effort: the role of interface faceting and grain boundary scattering. Because there is good experimental evidence that one of the principal properties of good epitaxial films is the relative smoothness of the metal/semiconductor interface, it appeared reasonable that an examination of the effects of the quality of the interface on scattering and the subsequent photoyield might prove revealing. An examination of the literature showed, however, that the standard treatment of interface scattering made certain simplifying assumptions. Modifications of the theory were required to take appropriate account of the effects of the quality of the interface. Specifically, it is usually assumed that hot electrons impinging on the interface are diffusely reflected (appropriate for a rough surface) but are transmitted over the interface as a whole into the silicon only within a narrow escape cone relative to the interface normal (appropriate for a smooth surface). It is our assessment that an interface which supports diffuse reflection (i.e., a rough surface) should also result in diffuse transmission

and that this may have an important influence on the photoyield. Secondly, the conventional theoretical treatments consider only isotropic scattering mechanisms, and thus the effects of grain boundary scattering have not been included in the theory. Our study was designed to extend the theory to take account of these effects.

2. Experimental Overview

In the experimental area, work began with a redesigned mask set (5058) which included test structures needed for the infrared photoresponse measurements, sheet resistance measurements and crystallographic characterization. Next, the e-beam evaporator used for the Pt deposition was retrofitted with a substrate heater needed to duplicate the PtSi fabrication process developed at RADC.

PtSi films fabricated on (111) and (100) Si showed uniform resistances and a general trend of increasing resistance with decreasing thickness from those of bulk values. This is expected, since surface effects at these thicknesses should increase resistance values. RED analysis of 80A single phase PtSi films grown on (111) Si has shown the films to be epitaxial with (020) PtSi plane parallel to the {111} Si plane.

Cross-sectional TEM and planar TEM work was done on PtSi films formed on (111) Si and (100) Si. A number of important microstructural and crystallographic observations were made on these films relevant to improving the quantum yield.

1. Both films were about 80A thick close to that expected for deposition of 40A of Pt.

2. Electron diffraction analysis shows that in both cases the silicide phase formed was orthorhombic PtSi which is the desired phase of the several Pt_xSi_y phases that can form.

3. PtSi on (111) Si is epitaxially related to the Si substrate. The orientation relationship is:

   (010) PtSi parallel to (111) Si for the film and wafer planes;
   [002] PtSi parallel to <220> Si in the plane.

   Three equivalent crystallographic variants of this orientation relationship are possible, and the PtSi film is composed of all three variants in apparently equal fractions.

4. PtSi on (111) Si nucleates and grows as islands; however, a continuous film is formed and is observed for films as thin as 20A. Impingement of boundaries of similar variants produces a larger interconnected grain structure than that which would be expected for island growth. Furthermore, an analysis of Moire fringe contrast indicates that the impingement boundaries between unlike variants have a high degree of lattice matching and are, therefore, low energy boundaries.

5. PtSi on (100) Si produces a near random, fine grain, polycrystalline film. A slight degree of preferred orientation is observed. Oblique views of cross-sectional specimens indicate that the grains of PtSi are thicker at the center than at the boundaries. Nonetheless, a fairly continuous film is produced.

6. No direct observation of the defect structure at the PtSi/Si interface was made. However, the interfacial roughness is less for PtSi/(111) Si than for PtSi/(100) Si. This observation is expected for an epitaxially related film versus a randomly related film. The epitaxial relationship of PtSi/(111) Si would suggest a lower energy interfacial structure than for randomly oriented PtSi (100) Si. Furthermore, the thickness uniformity of PtSi/(111) Si is better than for PtSi/(100) Si.

7. PtSi films of 20A formed on (111) Si were also epitaxial but exhibited strain from the hexagonal Si substrate.

8. Film coverages of 20A PtSi were better than 90% on (111) Si as determined by Moire Fringe patterns. This is different from island growth that was observed elsewhere[1].

9. Indirectly, these results show that the correct care was taken in the preparation of the wafer prior to the silicide formation and that the O_2 partial pressure was kept below levels inhibiting PtSi formation.

Four lots of PtSi/Si IR devices (lot #6039, 6180, 6184) fabricated at ATL and one lot fabricated during the program with variations in substrate orientation, PtSi thickness, anneal temperature and evaporation pressure. Devices from these lots were used for measuring IR response for the 2μ to 5.5μ band.

IR response and leakage measurements showed several features.

1. In general, no improvement in the response signal was observed for PtSi films of the same thickness formed over (111) Si versus (100) Si.

2. Curvature was observed on Fowler plots of 80A PtSi films on (100) Si and (111) Si for photon energies near the barrier value. This curvature disappears as the PtSi film thickness is decreased.

3. The extrapolated Schottky barrier value is reduced and the C_1 coefficient is increased as the PtSi thickness is reduced for both substrate orientations. On (111) Si the barrier changes from ~.3eV to .225eV and the C_1 coefficient is increased roughly a factor of 4 to ~19%/eV as the PtSi thickness is reduced from 80A to 10A.

4. At .5 volt reverse biased, the lowest leakage values were $\sim 10^{-8}$ amps/cm^2 when measured cold shielded and operated at 77K. However, all the diodes exhibited a soft breakdown with the typical leakage at 3 volts reverse bias of $\sim 10^{-5}$ amps/cm^2.

III. PROGRESS ANALYSIS

A. Theoretical Study

1. Introduction

The objective of our theoretical modeling effort is to build on the observed relationship between quantum efficiency enhancement and improvements in silicide epitaxy, relating the critical parameters in the theory of photoemission to experimentally measured parameters which characterize the silicide, such as degree of expitaxy, grain size, and defect density.

Our approach to the problem was guided by the experimental results of McKee[2] on Pd_2Si, and in-house VLSI work on silicides and information obtained from the literature on epitaxial silicide formation. McKee showed that Schottky barrier diodes of Pd_2Si formed on (111) Si had a factor of 2 photoyield enhancement over these with Pd_2Si formed on (100) Si. This coupled with evidence that silicides formed on (111) Si result in smooth metal/semiconductor interfaces while silicides formed on (100) Si result in facetted interfaced structures seemed to point out the importance of the silicide-silicon interface. Consequently, in this phase of the theoretical work, we focused on the effects of interface faceting on the photoyield. Our work builds on previous theoretical work, principally that of Vickers[3], but extending it to include the effects of interfacial faceting on hot-electron injection into the semiconductor.

Also developed, for the first time, are the effects of silicide grain boundary scattering on the photoyield. Our treatment of grain boundaries was guided by VLSI studies on thicker (1000A) silicide films and theoretical work used in the analysis of the electrical resistivities of thin films. Grain

boundary effects will not be presented here but are explained in detail in our first Quarterly Report. The following sections outline our analysis of interfacial scattering effects, and contains a summary overview and the conclusions of our work.

Interfacial roughness or the degree of faceting of a thin PtSi film is expected to vary as the silicon substrate orientation is changed from (100) to (111). Cross-sectional TEM photographs of $NiSi_2$ (1000A film, CaF_2 cubic structure) grown on (100) and (111) Si shows large scale (111) type faceting on the (100) substrate. Faceting does not occur on the (111) substrate. Both films are locally well defined, but the faceting on the (100) substrate demonstrates the stability of the (111) - type $NiSi_2$-Si interface over the (100) type interface[4].

It is also known[4] that PtSi and Pd_2Si grow pseudoepitaxially on (111) Si and that a similar instability for (100) type silicide - Si interfaces has been observed for PtSi and Pd_2Si[5,6]. Thus, even though PtSi (orthorhombic) and Pd_2Si (hexagonal) have different crystal structures than $NiSi_2$, it is reasonable to expect a more stable and thus less interfacial faceting for a PtSi (or Pd_2Si) film grown on a (111) Si substrate than on (100) Si.

Background on Interfacial Scattering

The major theoretical works on photoemission as represented by that of Vickers[3] and that of Dalal[7] are semiclassical, ballistic treatments which take into account multiple electron scattering at the metal boundaries and multiple internal scattering by cold electrons, phonons, and bulk point

defects. Diffuse reflections at the metal boundaries are effective in redirecting electrons outside of the escape cone into it and results in a photoyield enhancement with film thinning. For film thickness of the order of the hot electron mean free path, both models yield the same results, while for very thin films there are significant differences. Perhaps the major difference between the Vickers and Dalal treatment is that Dalal's is a one dimensional model while Vickers' model take account of the motion of hot electrons in three dimensions. An important addition to the theory was made by Mooney and Silverman[8], who extended Vickers model to include the effects of energy losses during scattering which are especially critical for very thin films.

The point of departure of our work from these theories is the treatment of electron scattering at the metal/semiconductor interface. Both Dalal and Vickers assume that hot electrons reflected from the interface are reflected randomly while those that are transmitted are transmitted only if they are directed within a narrow escape cone (where the escape cone axis is parallel to the nominal surface normal). It is our assessment, however, that an interface which supports diffuse reflection may also result in diffuse transmission. By developing a simple model to represent the interface scattering processes, we find that diffuse transmission has a significant effect on the photoyield.

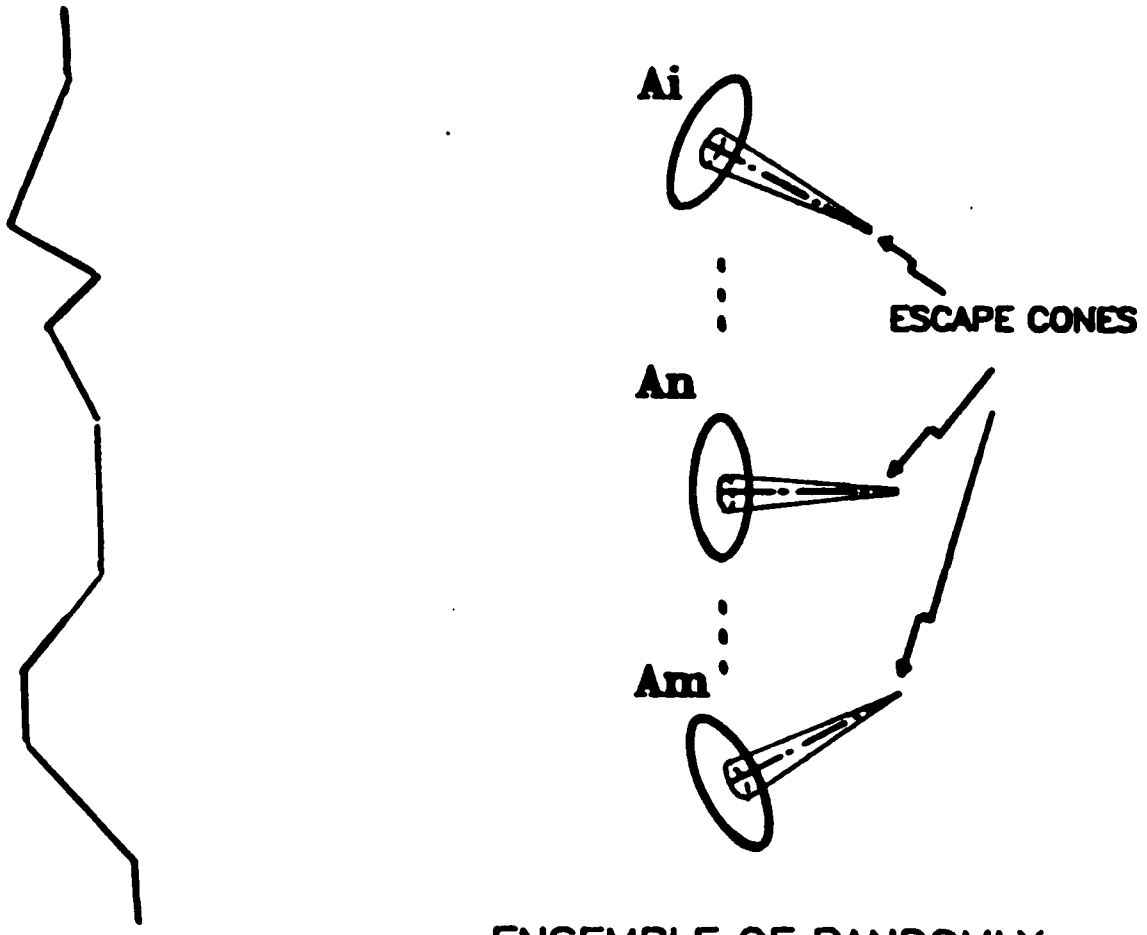
2. The Metal/Semiconductor Interface

A surface that supports diffuse scattering may be represented by an irregular surface which has variations in height that are large compared to the scattered electron wavelength[9]. While the electrons are scattered

locally specularly, the diffuse scattering property of the surface on a macroscopic level arises from random variations in the local surface normal. To a first approximation we may represent the interface by an ensemble of elemental plane surfaces the diameter of which is large compared to the scattered electron wave length. In such a picture a perfectly smooth interface is represented by an ensemble of elemental surfaces with all of the surfaces' normal parallel to the nominal surface normal and a perfectly rough surface by an ensemble whose surfaces' normal are oriented randomly (see Figure III-1).

An important feature of this representation is that, for electron scattering from an elemental surface the concept of an escape cone is maintained and the net effect of the variation of the orientation of the elemental surfaces is that the axis of the escape cone varies randomly over the surface. This leads to the properties of diffuse reflection and diffuse transmission.

INTERFACE MODEL

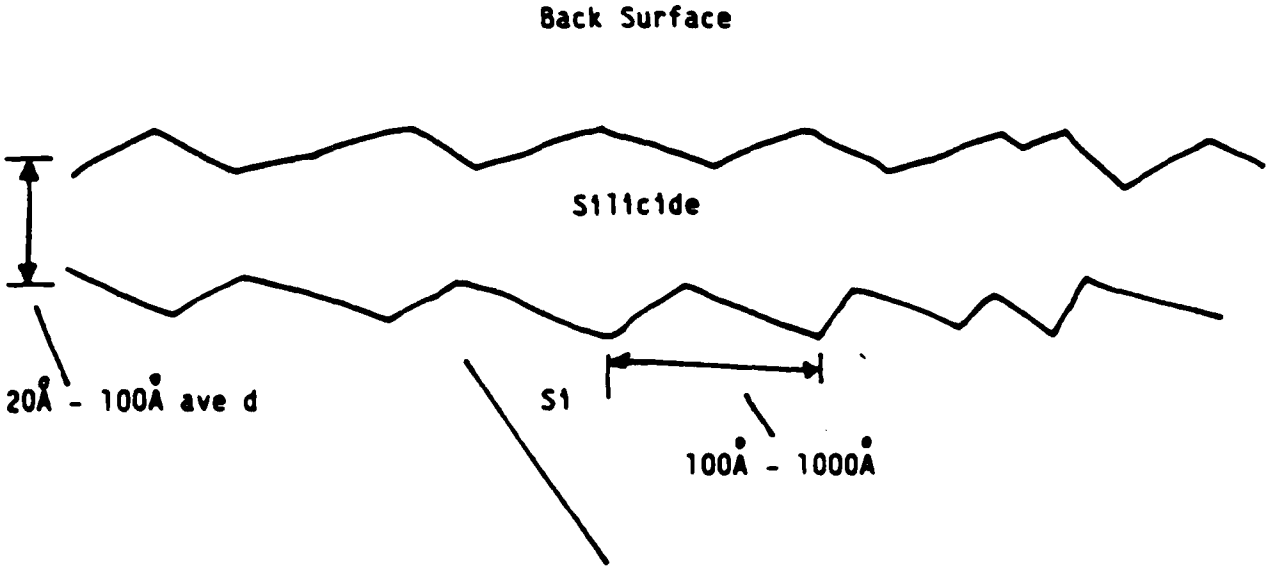


FACETTED INTERFACE

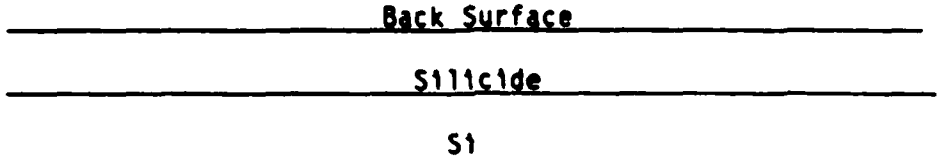
ENSEMBLE OF RANDOMLY ORIENTED ELEMENTAL SURFACES

Figure III-1 - Interface Model

Shown in Figure III-2 are the interface models for silicide film grown on either (100) or (111) Si substrate.



(100) Interface Model



(111) Interface Model

Figure III-2

3. The Photoemission Calculation

Using these concepts and the formulation of the photoemission problem as developed by Vickers, one can simply compute the effect of the diffuse transmission on the photoyield. Before outlining our approach, we briefly summarize the main features of Vickers' model.

In his formulation of the photoemission problem, Vickers computes the internal quantum yield by:

- First computing the probability that hot electrons may be transmitted from the metal into the semiconductor without being scattered. The result is summed to give a first order magnitude of the photoyield.

- Then taking into account the effects of internal scattering (taken to be elastic and isotropic). The net result of internal isotropic scattering is a replenishment of the original hot-electron distribution. The final photoyield is given by the first order expression multiplied by an isotropic scattering gain factor.

Figure III-3 outlines schematically the different paths a hot electron may take within the metal before injection into the semiconductor. From Figure III-3, one notes that electrons are transmitted into the semiconductor through the interface only if they are directed within a small angle about the surface normal. Electrons not within the escape cone of the nominal surface (path represented by ρ_α in the figure) are randomly reflected from the front and back surfaces until they are redirected into the escape cone or collide either with a cold electron or phonon.

Using d as the film thickness and Le and Lp as the electron-electron and electron-phonon mean free paths respectively, one can derive:

α, the probability that a hot electron will reach the interface from any point within the metal, travelling along the interface normal without scattering as:

$$\alpha = \frac{1}{d}\int_0^d \exp(-x/L^*)dx; \text{ where } \frac{1}{L^*} = \frac{1}{L_e} + \frac{1}{L_p};$$

β, the probability that a hot electron outside the escape cone will reach the interface from any point within the metal without being scattered as:

$$\beta = \frac{1}{d}\int_0^d \int_0^{\pi/2} \exp(-x/L^* \cos\theta)\sin\theta\, d\theta\, dx;$$

δ, the probability that a hot electron travels from one surface to another without being scattered as:

$$\delta = \int_0^{\pi/2} \exp(-d/L^* \cos\theta)\sin\theta\, d\theta;$$

b_f, the probability that a hot electron travels along a normal path from the back surface to the front without being scattered as:

$$b_f = \exp(-d/L^*)$$

ELECTRON TRAJECTORIES WITHOUT INTERNAL SCATTERING

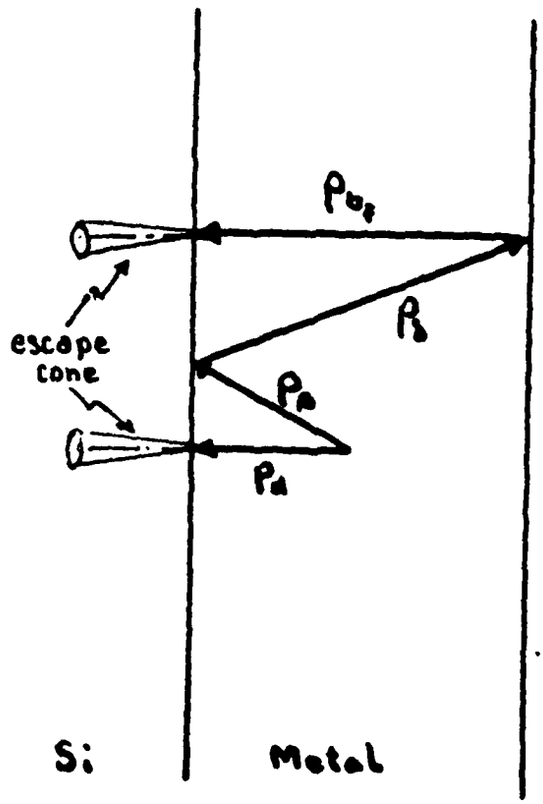


Figure III-3

(1289H)

An expression for the first order photoyield is obtained by computing the probability that a hot electron may reach the interface directed along the surface normal (i.e. within the surface escape cone) by summing over all the ways it may reach the interface without being scattered internally by a phonon or a cold-electron. The sum of these probabilities is $\bar{U}\ (d/L^*)$ where:

$$\bar{U}\ (d/L^*) = \alpha + e^{-d/L^*}\ \beta(1 + \delta + \delta^2 + \delta^3 + \ldots)$$

and the power series in δ represents multiple reflections at the metal boundaries.

Internal scattering is taken into account by noting that after each isotropic, elastic scattering event, the scattered hot electron distribution resembles the original distribution except that it is only γ times as large as the original. γ is the probability that a hot electron has collided with a phonon before collison with a cold electron. Thus γ is given by:

$$\gamma = \int_0^\infty \exp\ (-x/L^*)\ \frac{dx}{L_p} = \frac{L_e}{L_e + L_p}$$

and the isotropic scattering replenishment factor is:

$$1 + \gamma + \gamma^2 + \gamma^3 + \ldots = \frac{1}{1 - \gamma}\ .$$

The expression for the total photoyield is:

$$Y = Y_F\ \frac{L^*}{d}\ (1 - \gamma)^{-1}\ U(d/L^*) = Y_F\ \frac{L_e}{d}\ U(d/L^*)$$

where Y_F = Fowler/Archer Photoyield Expression

and $U(d/L^*) = d/L^*\ \bar{U}(d/L^*)$

The modification that our treatment offers is that the escape cone is now defined relative to elemental surfaces which are randomly oriented over the interface as a whole. Electrons may escape now through any angle. The net effect may be taken into account in Vickers formulation with a simple transformation of his escape probability terms. Namely,

the α term transforms into a β term

and the e^{-d/L^*} term transforms into a δ term.

The final expressions for the internal photoyield are given by:

$$Y_{specular} = Y_F \frac{Le}{d} (1 - e^{-2d/L^*})$$

$$Y_{diffuse} = Y_F \frac{Le}{d} \frac{\beta}{1 - \delta}$$

Figures III-4 and III-5 compare the results of our calculations for a smooth (i.e., specular scattering) interface and a facetted interface (i.e., diffuse scattering) with those of Vickers. The principal feature of our calculation is that it shows that for large values of the parameter d/L^*, diffuse transmission of hot electrons at the metal/semiconductor interface degrades the photoyield by a factor of 2 below that for a smooth interface and enhances the photoyield over that of a smooth interface for very small values of d/L^*.

PHOTOYIELD U-FUNCTIONS

COMPARISON OF VICKERS AND PRESENT THEORY

DIFFUSE — — VICKERS ——— SPECULAR ——·——

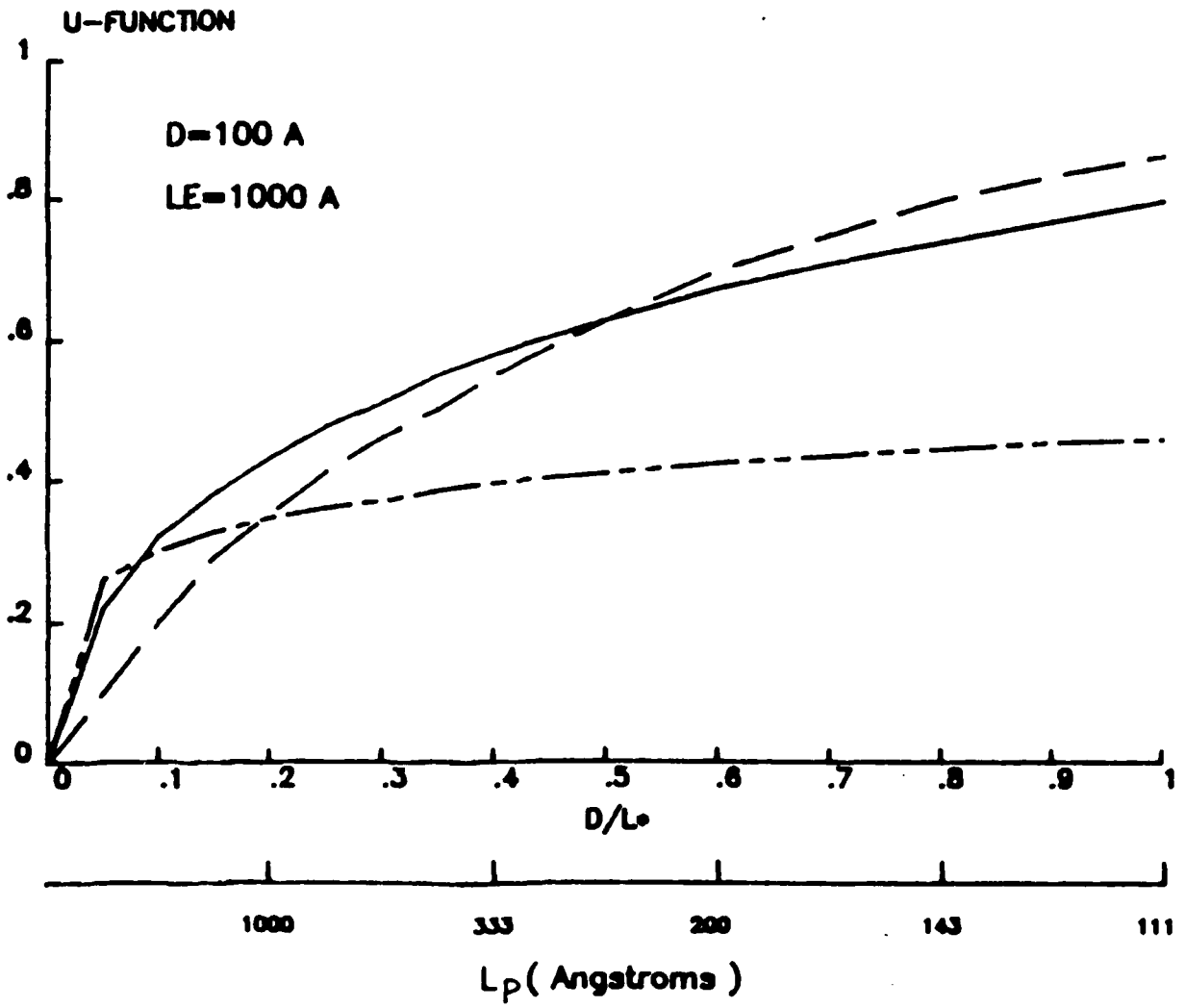


Figure III-4 -

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PHOTOYIELD U-FUNCTIONS

COMPARISON OF VICKERS AND PRESENT THEORY

DIFFUSE VICKERS SPECULAR

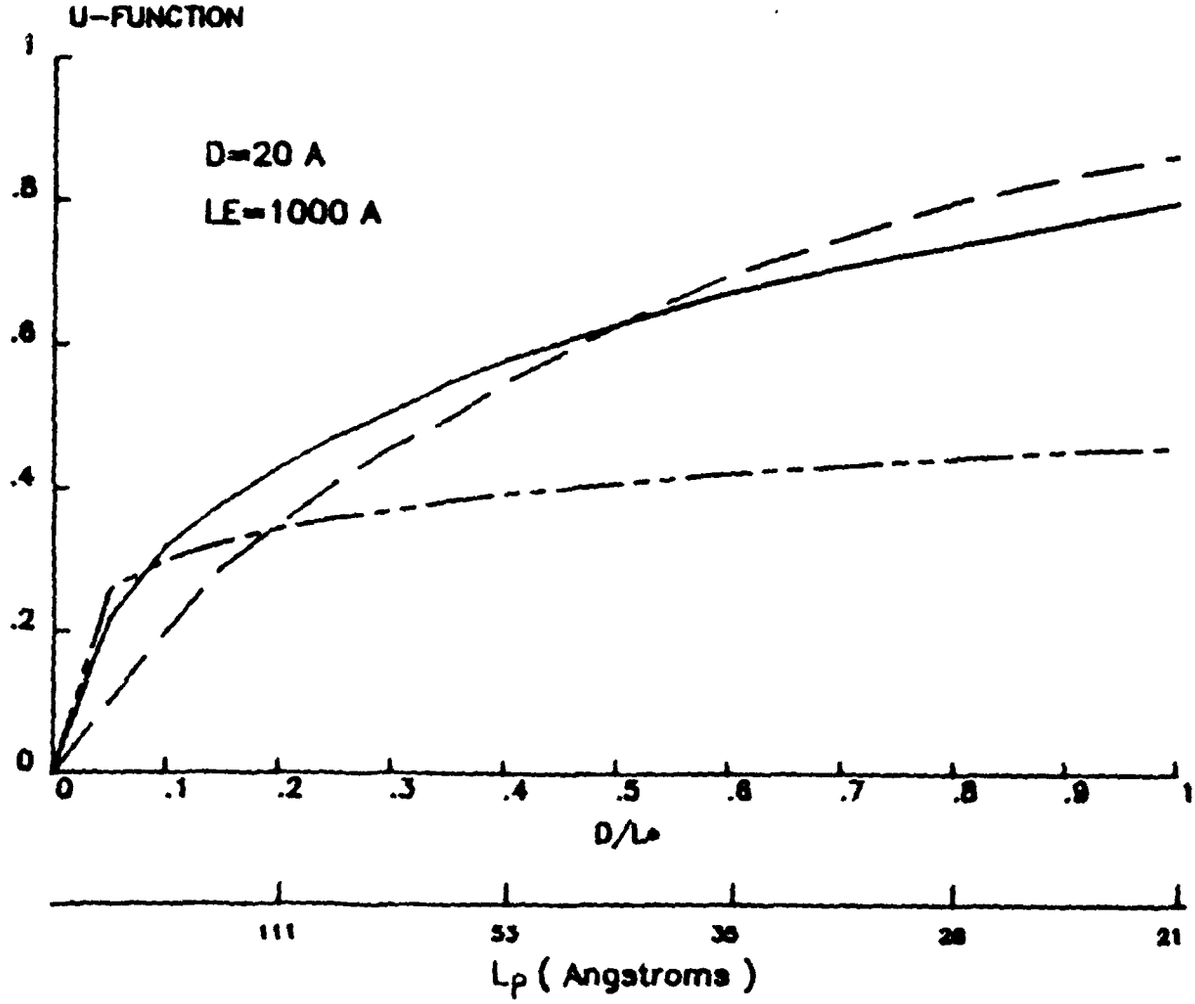


Figure III-5 -

B. Experimental Progress

This subsection describes the experimental work performed toward meeting the contract's objective more or less chronologically. Generally, work which has not been previously reported in the Interim report will be explained in greater detail. However, TEM and response data will be presented in detail.

As in the Interim report a crystallographic notation list, which will be used in the report is provided as follows:

< > ≡ equivalent directions

[ ] ≡ specific directions

{ } ≡ equivalent planes

( ) ≡ specific planes.

Also, henceforth, PtSi will be used to designate the silicide with the understanding that the phase is orthorhombic PtSi. The crystallographic axes of the orthorhombic PtSi will be that used by the ASTM Joint Committee on Powder Diffraction Standards (JCPDS) power diffraction file 7-251; i.e., a_o = 5.932 A, b_o = 5.595 A and c_o = 3.603. All orientation relationships will be reported using these axes. Other designations have been used in the literature.

The initial work of the redesign of the 1716 mask set heretofore called the 5058 mask set and e-beam Pt evaporation modification was described in the Interim report and is not repeated here.

1. Resistivity

Resistance values of PtSi films annealed at various temperature and thicknesses on blank control wafers over several runs were measured. This data is presented in Table III-1 and graphed in Figure III-6.

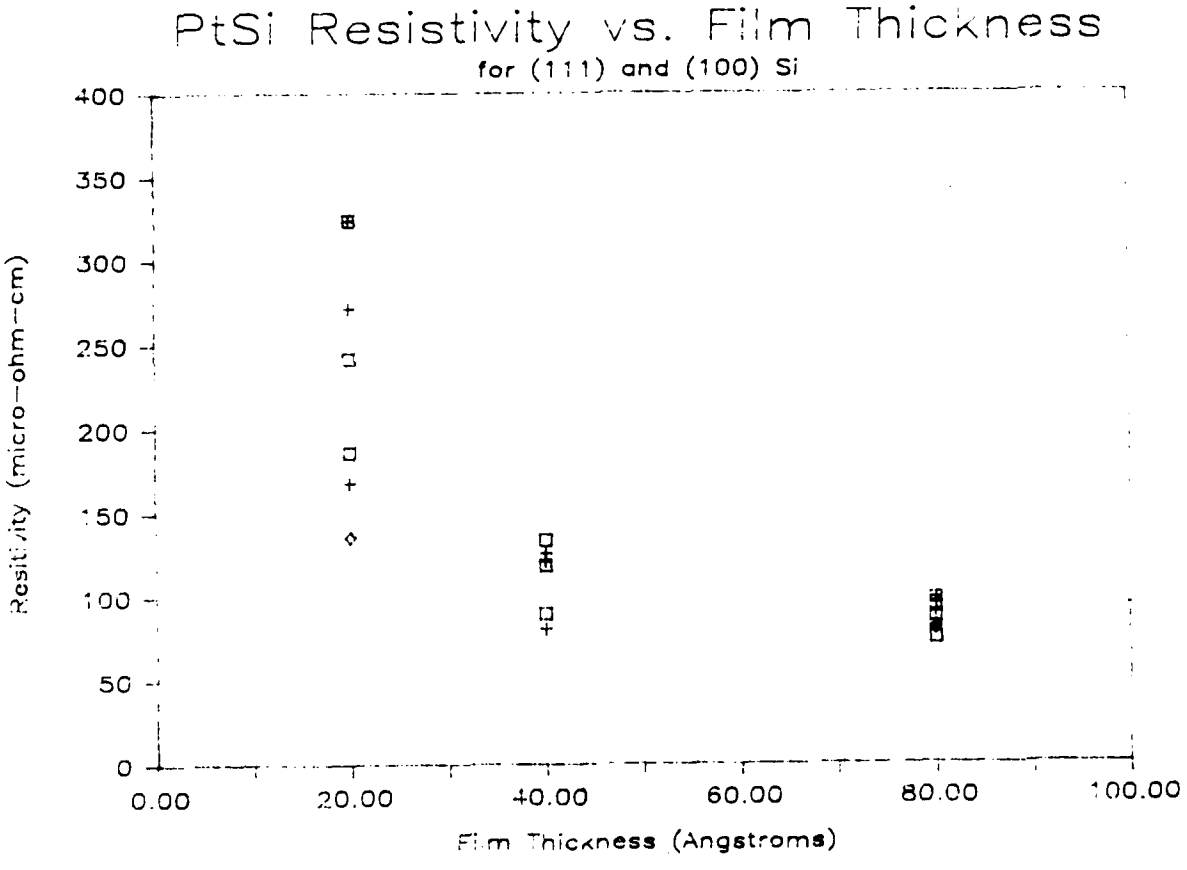


Figure III-6

(1289H)

TABLE 1

Wafer #	ρ_b (μΩ-cm)	ρ_a (μΩ-cm)	σ a (% across wafer)	
111-1	81.4	87.4	1.6	
111-2	95.9	97.9	4.0	
111-3	80.1	74.3	1.3	
100-1	80.5	79.5	1.9	
3-111-1	98.3	92.6	2.6	
3-111-2	90.1	86.7	1.9	
4-111-1	121.5	134.1	25.5	(broken wafer)
4-111-2	126.4	118.6	4.4	
5-111-1	272	242	9.1	
5-111-2	168	186	3.1	
6-111-1	324	324	1.5	
6-100-1	136	136	13.4	
8-111-1	81	90	2.4	

$\rho_b \equiv$ before Pt strip and/or 400°C H_2 anneal

$\rho_a \equiv$ after Pt strip and any 400°C H_2 anneal

Wafer #	Wafer History
111-1	~ 40A Pt deposition, (111) wafer, run #2.
111-2	Same.
111-3	Same plus a 1/2 hour 400°C H_2/N_2 anneal before Pt strip.
100-1	Same as 111-3 only (100) wafer.
3-111-1	40A Pt deposition, (111) wafer, anisotropically etched, run #3.
3-111-2	Same, only no anisotropic KOH etch.
4-111-1	~ 20A Pt deposition (111) wafer, substrate was not outgassed during Pt deposition, run #4.
4-111-2	Same.
5-111-1	~10A Pt deposition (111) wafer 5 hour 425°C anneal.
5-114-2	Same
6-111-1	10A Pt on (111) Si - 5 hour, 425°C anneal
6-100-1	10A Pt on (100) Si - 5 hour, 425°C anneal
8-111-1	20A Pt on (111) Si - 5 hour, 425°C anneal

(1289H)

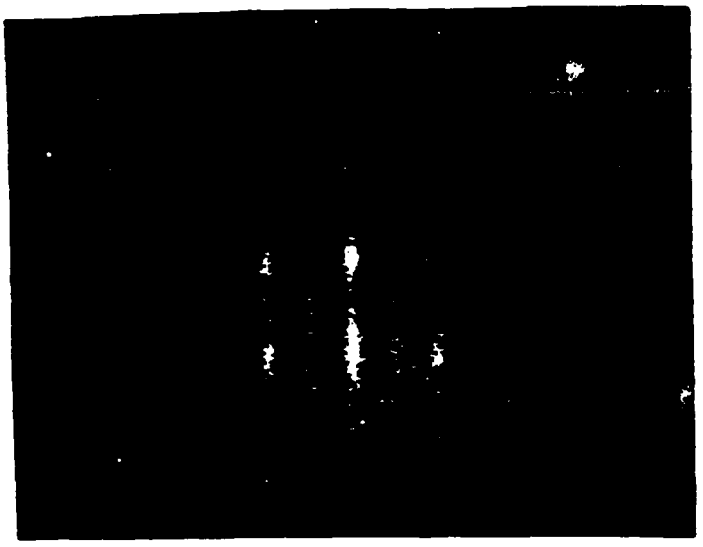
Trends in the data include a definite increase in sheet resistivity upon a decrease in Pt thickness. This is expected since surface effects raise the resistivity values from the bulk value, which is ~35-40 $\mu\Omega$-cm[10]. Generally, there was little or no change upon Pt stripping.

RED studies were next performed on wafers 3-111-2 and 100-1. Using 100 KeV electrons, RED patterns for two perpendicular Si orientations of wafer 3-111-2 are given in Figure III-7. These patterns indicate a good epitaxy of orthorhombic PtSi on Si. The planar relationship is (020) PtSi parallel to (111) Si. The PtSi phase is the only phase identified from the diffraction pattern. Pt, Pt_2Si and $PtSi_2$ structures were not detected in the RED analysis. Lattice constants of orthorhombic PtSi were determined to be 5.595A, 3.603A and 5.932A.

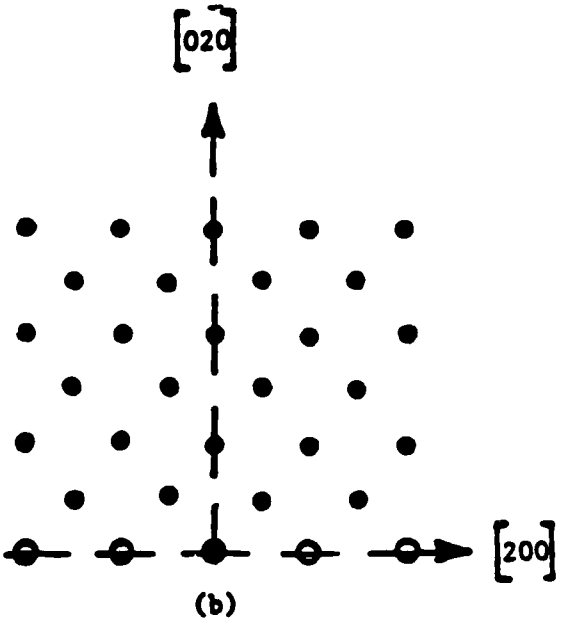
Crystallographic Analysis

The crystallographic analysis includes Reflection Electron Diffraction (RED), cross-sectional and planar Transmission Electron Diffraction (TEM) on sample films 20 - 80A thick fabricated at ATL. Next, the crystallographic qualities of films fabricated at the Pittsburgh R&D Center are discussed. The MBE/UHV facility has a variety of diagnostic equipment, which include in situ use of XPS, LHEED and RHEED. Auger analysis was also performed on ATL films but has already been presented in the Interim Report.

The PtSi unit cell and the unit cells atoms projections onto the {020} plane are shown in Figures III-8 and III-9. Shown in Figures III-10 and III-11 are the Si cell structures and its projection onto the {111}

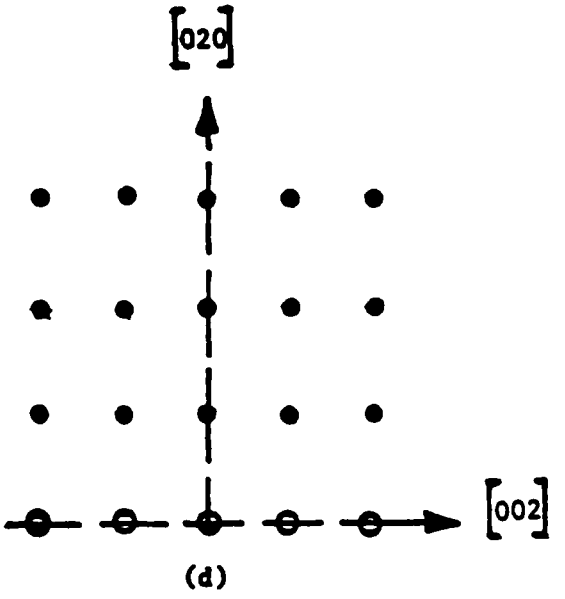


(a)



(b)

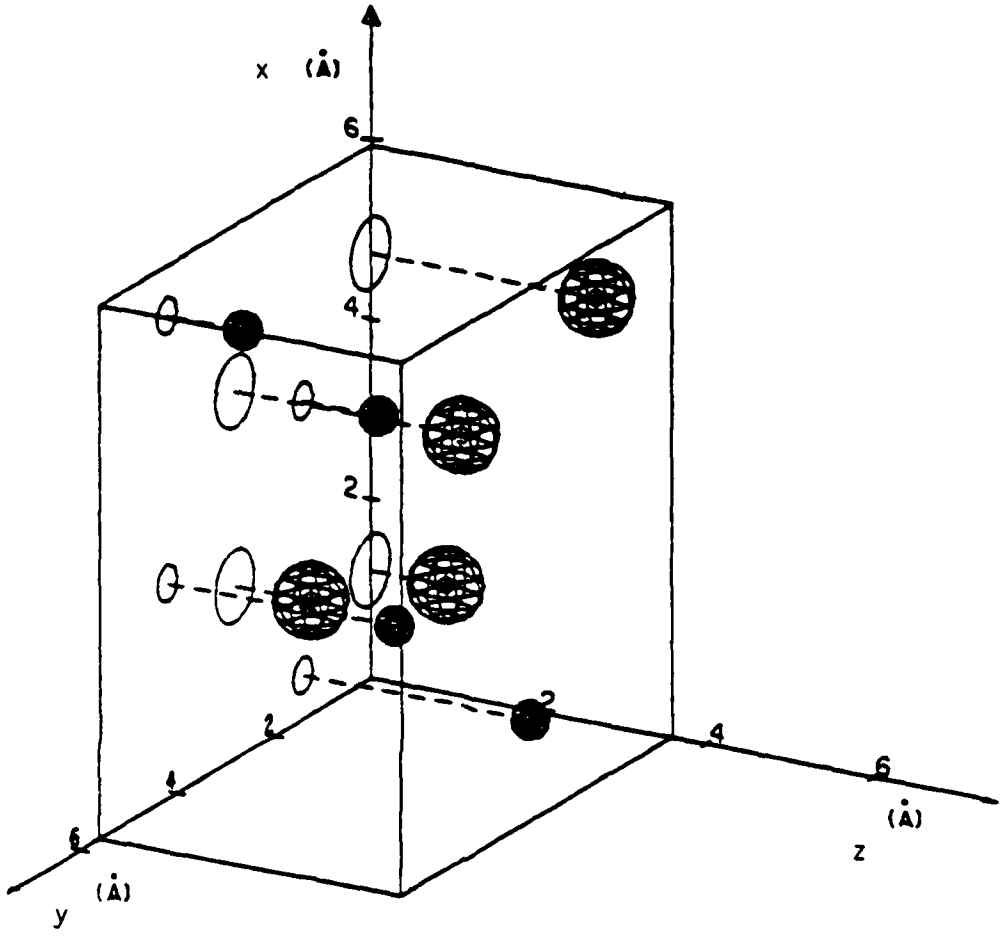
(c)



(d)

Figure III-7

Electron diffraction patterns from orthorhombic PtSi films. Actual patterns from {020} planes parallel to {111} Si are shown in (a) and (c). Figures (b) and (d) are idealized diffraction nets for the former.



≡ Pt atoms

≡ Si atoms

Figure III-8

Three-Dimensional Projection of the PtSi Orthorhombic Unit Cell

(1289H)

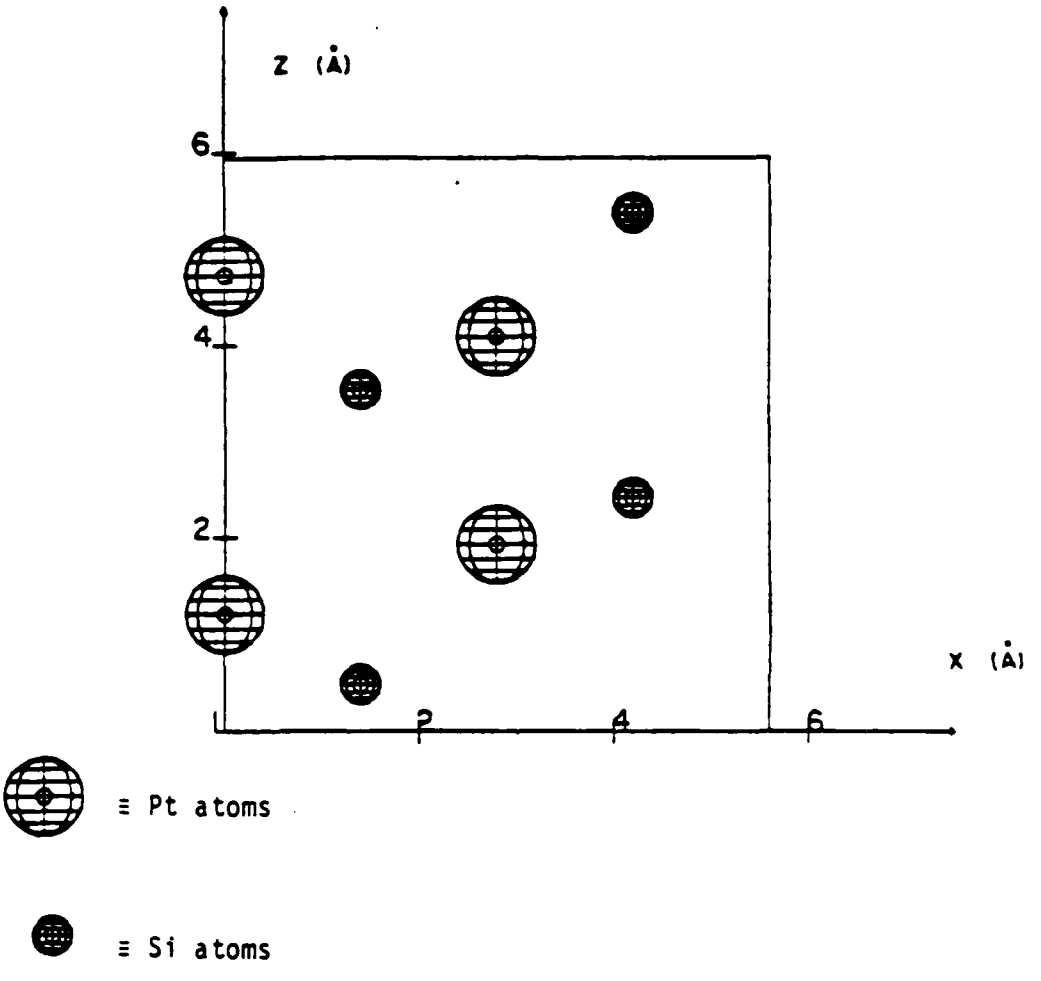


Figure III-9

Projection of the Orthorhomic PtSi Unit Cell onto the (020) Plane

(1289H)

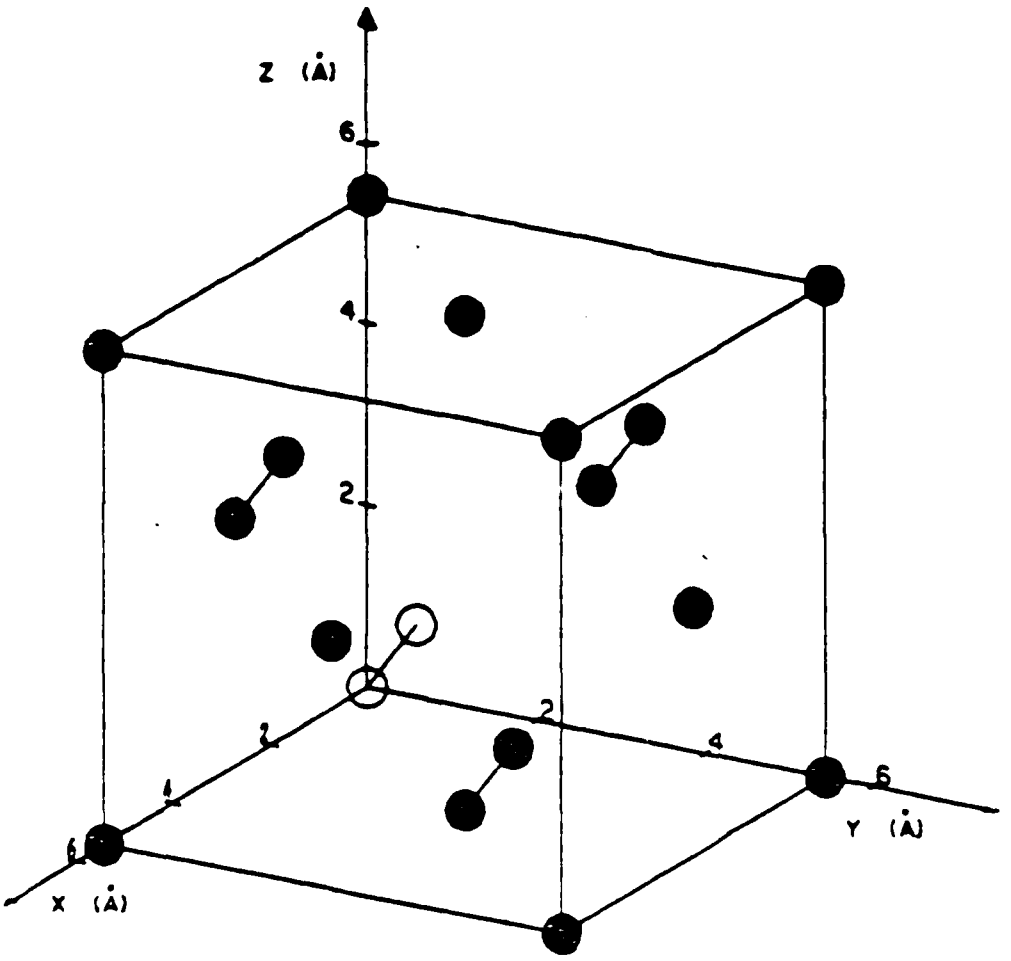


Figure III-10

Three-Dimensional Projection of the Si FCC Diamond Structure

(1289H)

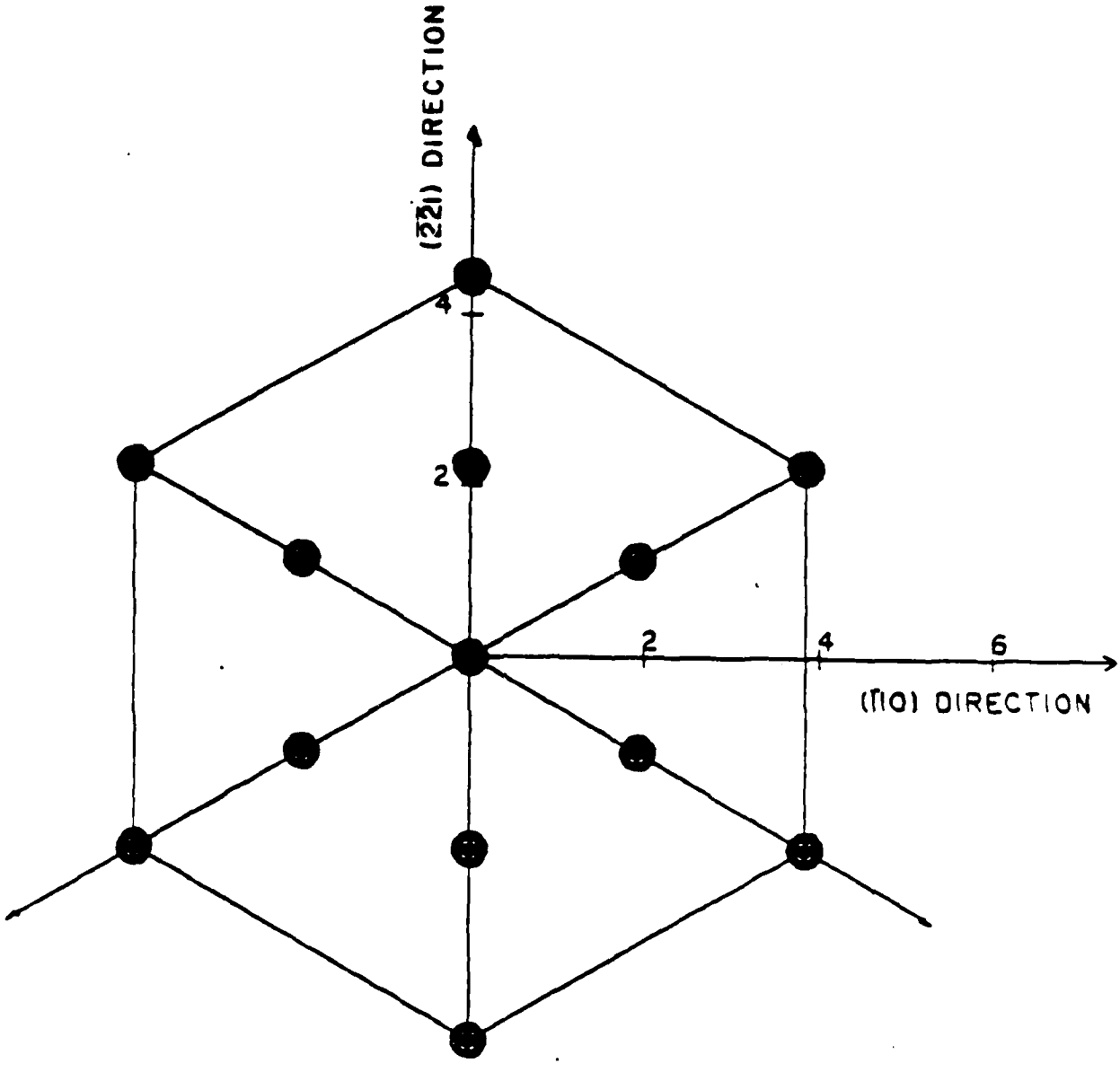


Figure III-11

Projection of Cubic Si Atoms Onto the (111) Plane
Showing Hexagonal Symmetry

(1289H)

plane. Planar TEM work completely identifies the epitaxial relationship with the PtSi {020} parallel to Si {111} (also observed elsewhere[11]), along with {100} PtSi // to {111} Si and {111} PtSi // {111} Si[11]. The orientation depends upon the anneal cycle.

Recently, in very high vacuum systems (2 x 10^{-10} torr deposition pressure) PtSi epitaxial formation of thin PtSi films (~160A) has also been observed on clean (100) Si[1]. RED analysis performed on wafer 100-1 showed no evidence of epitaxial PtSi formation on (100) Si, but later planar TEM showed this predominance of the PtSi phase and a slight preferencial orientation.

Planar and cross-sectional TEM studies were done on ~80A films formed on (111) Si and (100) Si and 20A PtSi films on (111)Si. These show planar PtSi layers regardless of the substrate orientation. However, epitaxial PtSi only forms on the (111) Si substrate.

Figure III-12 shows a cross-sectional TEM view of PtSi on (111) Si (wafer 3-111-1). This specimen is capped with amorphous Si layer for edge protection. The uniformity of the PtSi thickness is very good, varying from ~55A to 70A. Thickness monitor values for this run indicate an expected 80A PtSi film.

The Figure III-13 view is the same as Figure III-12, except the PtSi has been formed on (100) Si (wafer 100-1). Note that the PtSi/Si interface is more irregular than the top surface, and more irregular than the PtSi/Si interface on (111) Si in Figure III-12, but still has good uniformity. The silicides shown in Figures III-12 and III-13 were processed identically, but in different runs.

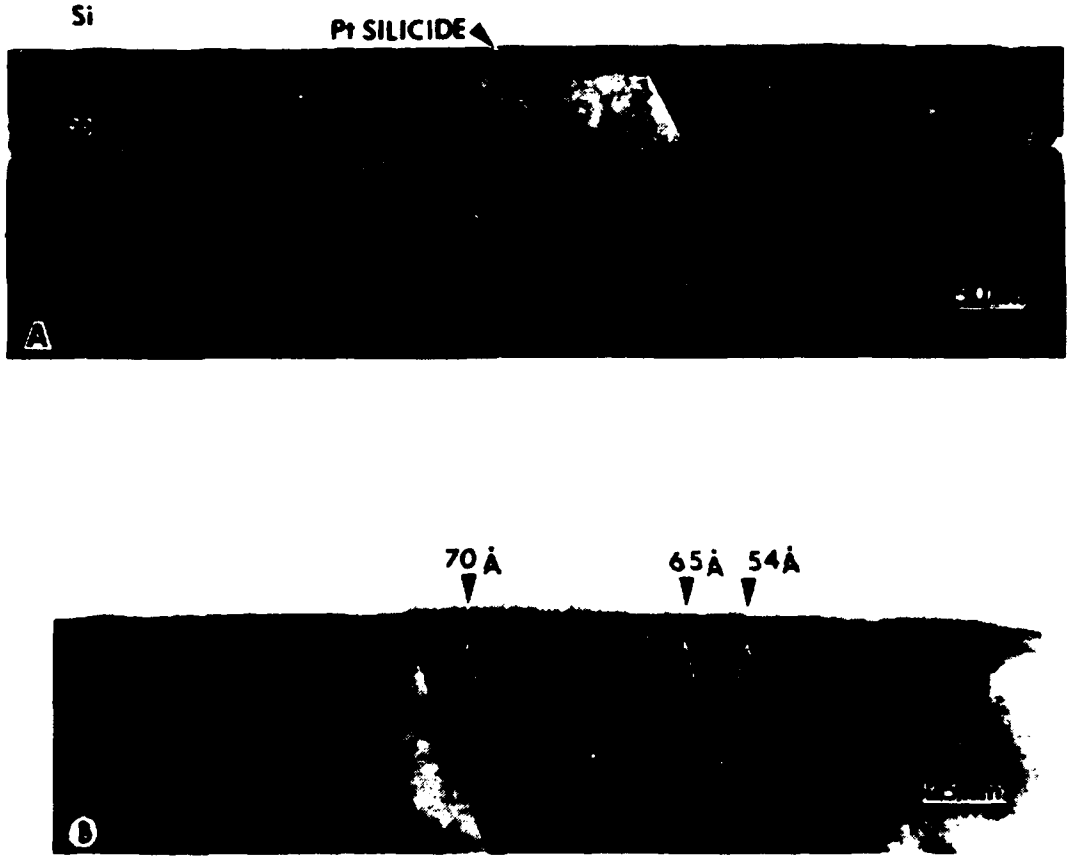


Figure A is a cross-sectional TEM photograph of a thinned (111) Si wafer having a thin reacted PtSi film with an expected thickness of 80A. This representative cross-section indicates the lack of substantial PtSi thickness variation. Figure B is a magnified view of Figure A.

Figure III-12

(1289H)

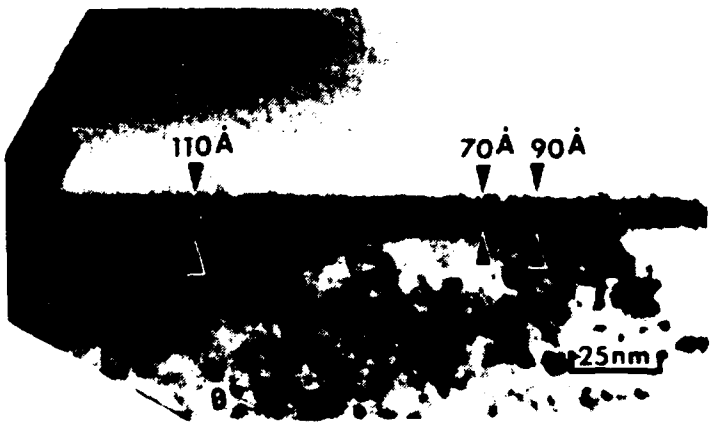


Figure A is a cross-section TEM photograph of a thinned (100) Si wafer having a thin, reacted PtSi film similar to Figure III-12. The (100) Si TEM photograph exhibits more PtSi film thickness variation than observed with films on (111) Si. Figure B is a representative enlargement of Figure A.

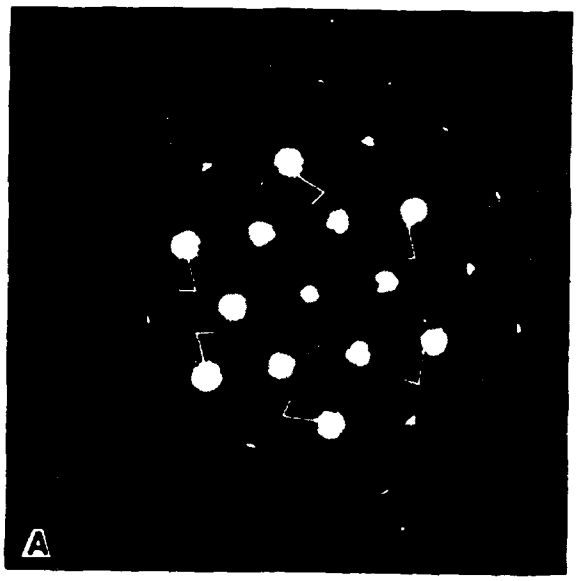
Figure III-13

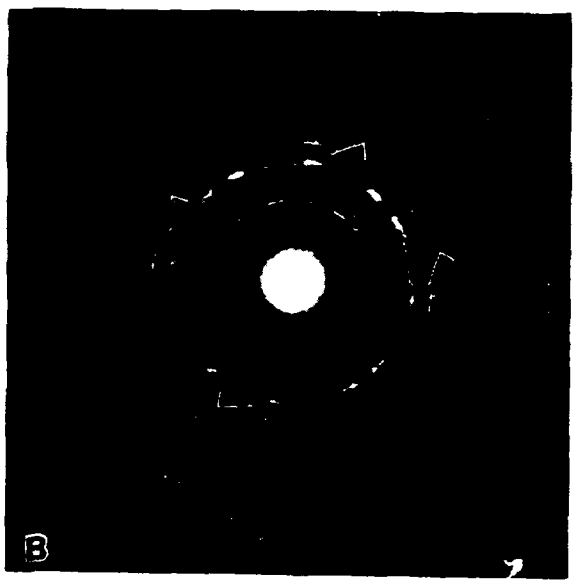
(1289H)

Figure III-14 shows electron diffraction patterns from planar TEM specimens of both types. Figure III-14A is the PtSi pattern plus a (111) Si pattern. The arrows mark the positions of Si (220) reflections with the remaining spots from an epi-PtSi. The PtSi orientation is that of a single main orientation with several variants leading to the side bands around the Si reflections and the multiple spots being from double diffraction, which is consistent with the RED results reported earlier.

Figure III-14B is from an unsupported PtSi film on (100) Si (all of the Si substrate has been chemically removed). This pattern is basically random with some slight preferred orientation (notice arcs). D-spacings confirm that PtSi is the dominant phase and that Pt, Pt_2Si, and $PtSi_2$ phase are not present. Arrows point to positions of previously underlying (100) Si, which lie close to the arcs. Figure III-14C shows both patterns from PtSi and from the (100) Si. Some double diffraction is evident. Patterns A, B and C in Figure III-14 are taken from large areas relative to the grain size. This emphasizes the fact that on (111) Si, all the PtSi is oriented with respect to the Si.

Figure III-15 shows bright field and dark field pairs from PtSi/Si substrate (111) (wafer 3-111-1) planar specimens. A and C are bright field images while B and D are dark field images. One of the (220) Si and PtSi side band reflections indicated in Figure III-14A were used to form the dark field images. Please note the Moire fringes. This effect occurs whenever two crystals of different lattice spacing overlap. The almost complete coverage of the micrograph by Moire fringes indicates very good coverage by the epitaxial PtSi. Some of the very dark small areas in the dark fields such as





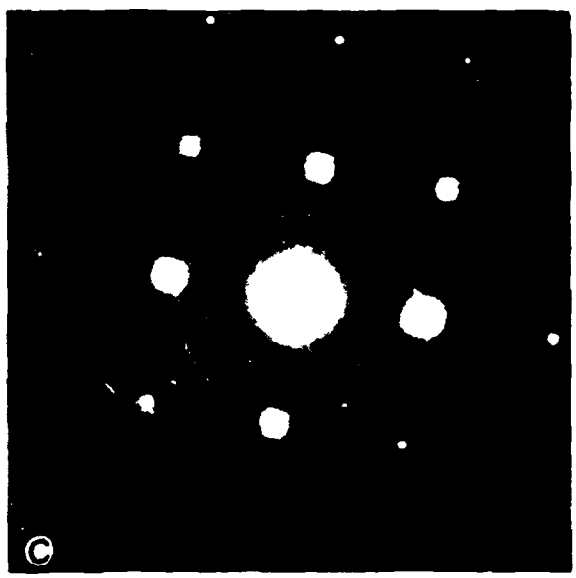


Figure III-14

Figures A, B and C are electron diffraction photographs for different orientation of PtSi film and the Si substrate. Figure A illustrates epitaxial PtSi with (111) Si. Figure B shows a suspended polycrystalline PtSi film originally formed on (100) Si. Figure C illustrates a polycrystalline PtSi film with the underlying diffraction pattern of the (100) Si substrate.

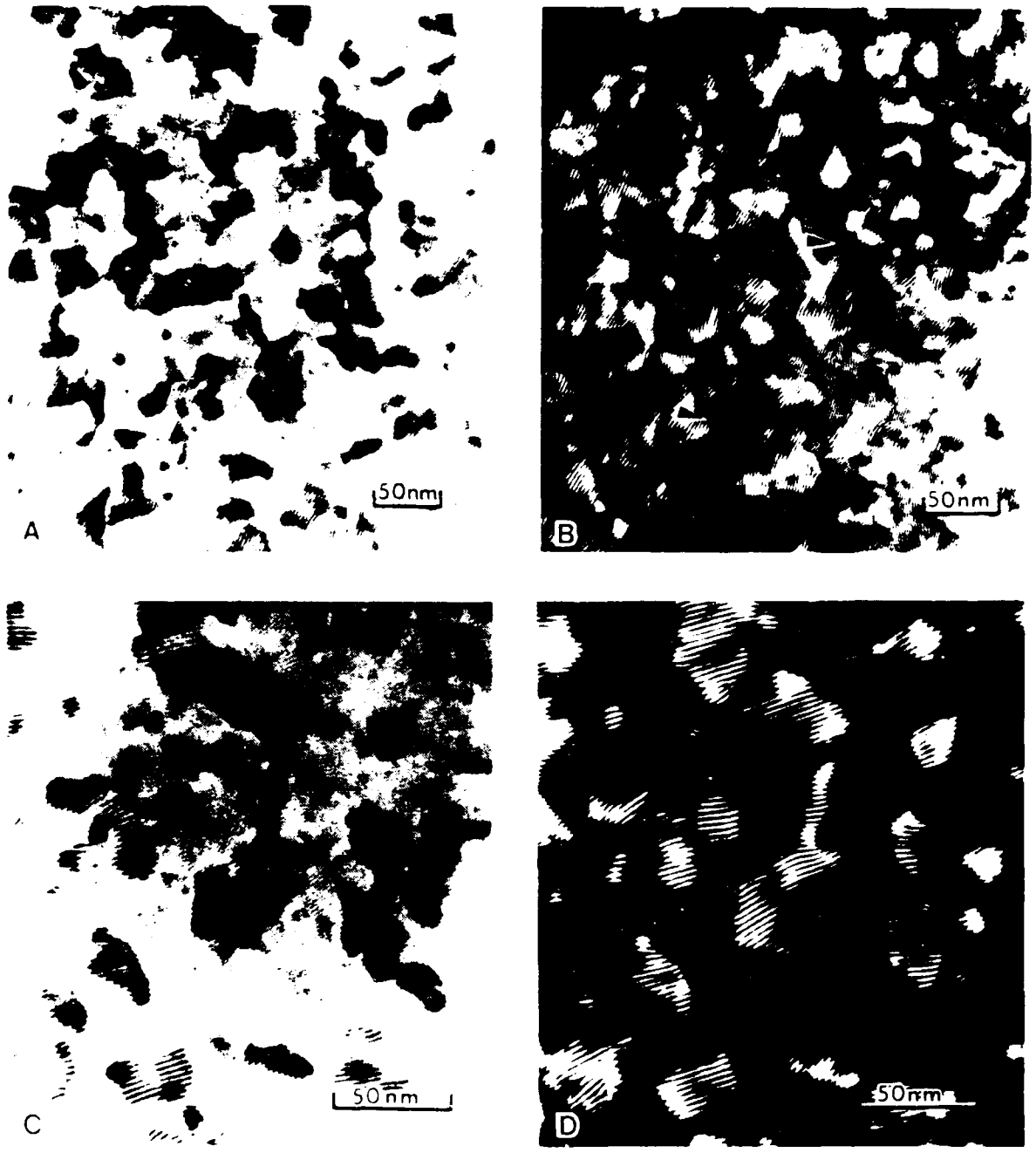


Figure III 15

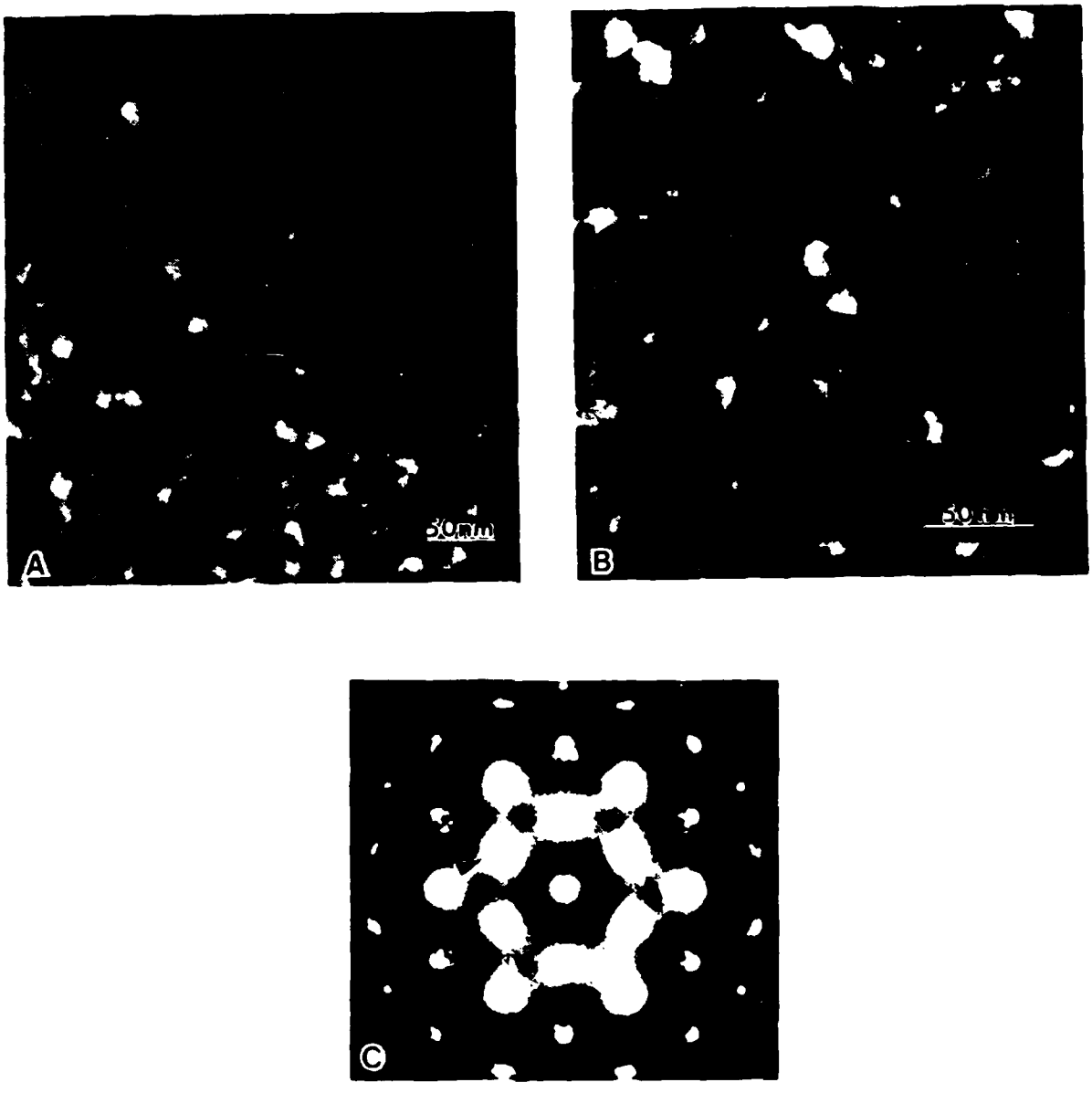
Bright field (A and C) and dark field (B and D) images of PtSi films on (111) Si. These images illustrate film grain boundaries and are formed from the adjacent diffraction spots [(220) Si and a PtSi side band] from the PtSi film and the Si. Notice the Moire fringes which indicated the extent of the epitaxial film coverage.

(1289H)

those indicated by the arrows in Figure III-15B, where no fringes exist, probably have no PtSi. The darker areas in the bright field (or light areas in the dark field) are from a variant (a rotated orientation) of PtSi and is explained more fully, later in the text. The other areas are from equivalent variants. Large and interconnected grains are apparent from these images and range in size from ~200A to 500A.

Figure III-16 illustrates dark field micrographs from one of the reflections of the type shown in C. Figures A and B are of different magnification (220,000X and 360,000X respectively) and show grain sizes of several hundred Angstroms. The electron micrographs of Figures A and B are formed from only PtSi reflections on (111) Si, no silicon reflections. Note that there are no Moire fringes, which is expected. The various shades of gray (bright areas) are from different variants of the silicide diffracting to various degrees. It is also apparent that there exists a high degree of interconnectivity of PtSi grains in both Figure III-16, A and B, and Figure III-15.

Figure III-17 illustrates bright field and dark field images from PtSi on (100) Si planar specimens similar to Figure III-15 (with the grain images from a Si and neighboring PtSi reflection in D). Notice the presence of some Moire fringes, but not to the extent as the PtSi on (111) Si. These grain sizes are generally slightly smaller and exhibit little grain interconnection as that observed in Figures III-15, 16.



Figures A and B are dark field TEM micrographs of PtSi [illegible] taken from the PtSi reflection arrowed in Figure [illegible] while the diameter of Moire fringe

Figure III 16

(1289H)

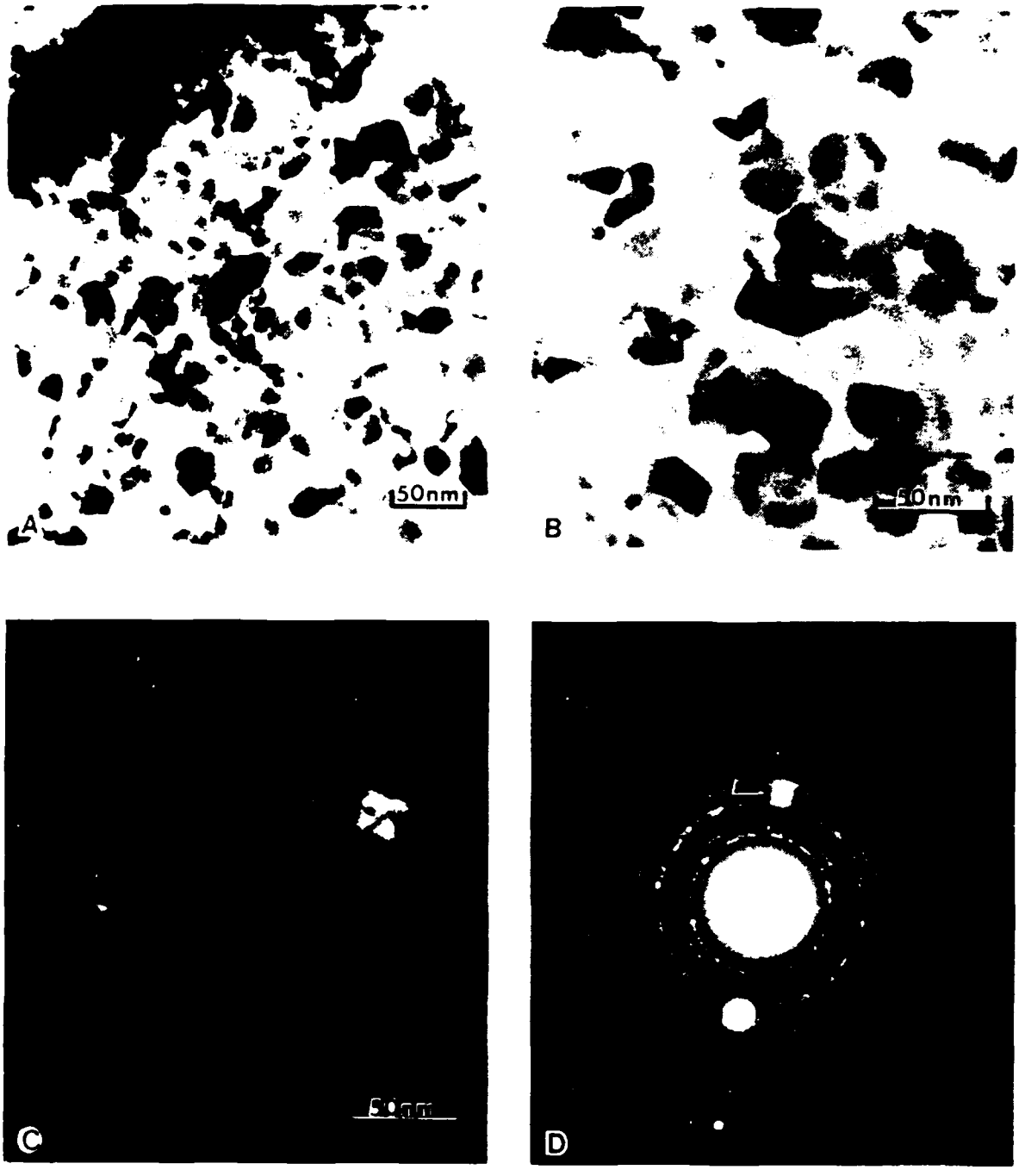


Figure III-17

Figures A and B are bright field TEM micrographs with different magnification of PtSi/(100) Si formed from the PtSi and Si reflection arrowed in Figure D. Figure C shows a dark field TEM micrograph of PtSi/(100) Si. Notice on Figures A, B and D the Moire Fringes on $\leq$ 5% of the area, indicating the general lack of epitaxial formation on the ($\bar{1}00$) Si.

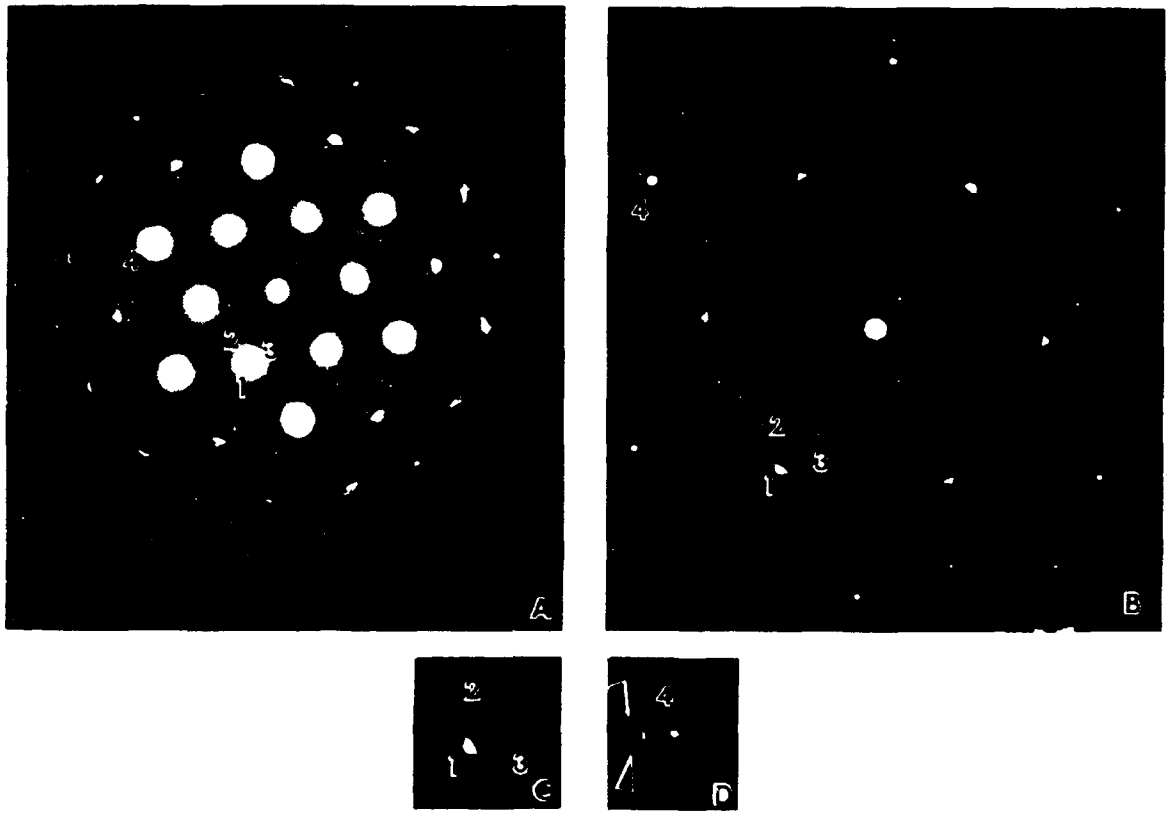
(1289H)

It has been determined from RED and planar TEM patterns that the (020) PtSi place is parallel to (111) Si. In order to completely determine the crystallographic orientation (and any variants) of orthorhombic PtSi film to the (111) Si wafer, a more detailed analysis must be performed from our planar TEM diffraction pattern. This has been done and is described in the following text.

Shown in Figure III-18A are diffraction pattern showing reflection from a <111> zone axis of Si and PtSi reflections. The inner reflections such as the ones marked 1, 2, and 3 are from PtSi. Reflections of the type marked 4 and highlighted in Figure III-18D are (220) type Si planes and sidebands. The sidebands indicate that a lot of multiple reflection is occurring.

Figure III-18B is the same pattern as A but at a high magnification. This pattern is taken with highly collinated beam to give good angular resolution and short exposure times in order to see distribution of intensities around each reflection. Note that reflections marked 1, 2 and 3 are actually multiple reflections as shown in C at higher magnifications. Each one is composed of a short streak and a long streak with 2 and 3 being weaker than 1 indicating that they occur by double diffraction.

Measurements of the spacings of the diffraction spots indicated the possibility that (002) PtSi was aligned along (220) Si with (200) or (101) PtSi at ~90° to this orientation. Shown in Figure III-19 is one side orientation. Large reflections (spots) are from a Si <T11> axis. Small reflections (spots) are from PtSi <010> (020) zone axis. (002) PtSi has been oriented parallel to (220) Si. Note the pseudohexagonal (distorted) nature of the PtSi reflections. This PtSi pattern may be rotated 120° so that (002) PtSi is along (220) Si and another 120° so that (002) PtSi is along (022) Si.



Figures A and B are diffraction patterns showing reflection from a <111> axis of Si and the PtSi reflections. In Figure B, the total exposure has been reduced, revealing diffraction pattern detail about the main pattern. Figure C shows PtSi reflections, while Figure D highlights reflections from (220) Si planes and side bands.

Figure III-18

(1289H)

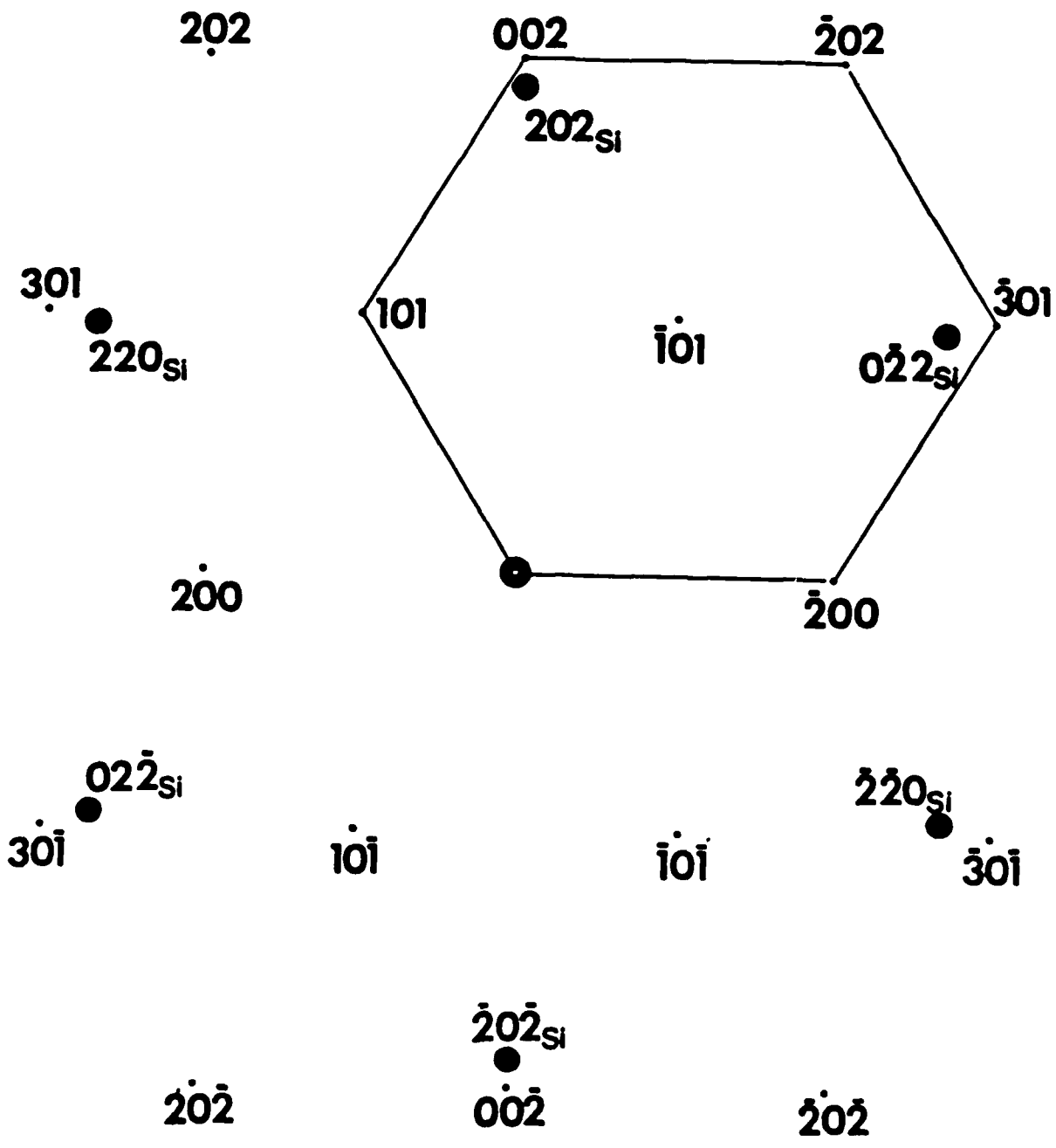


Figure III-19

The above diffraction pattern would occur if (002) PtSi was oriented parallel to (220) Si. Note the pseudohexagonal pattern which is produced.

(1289H)

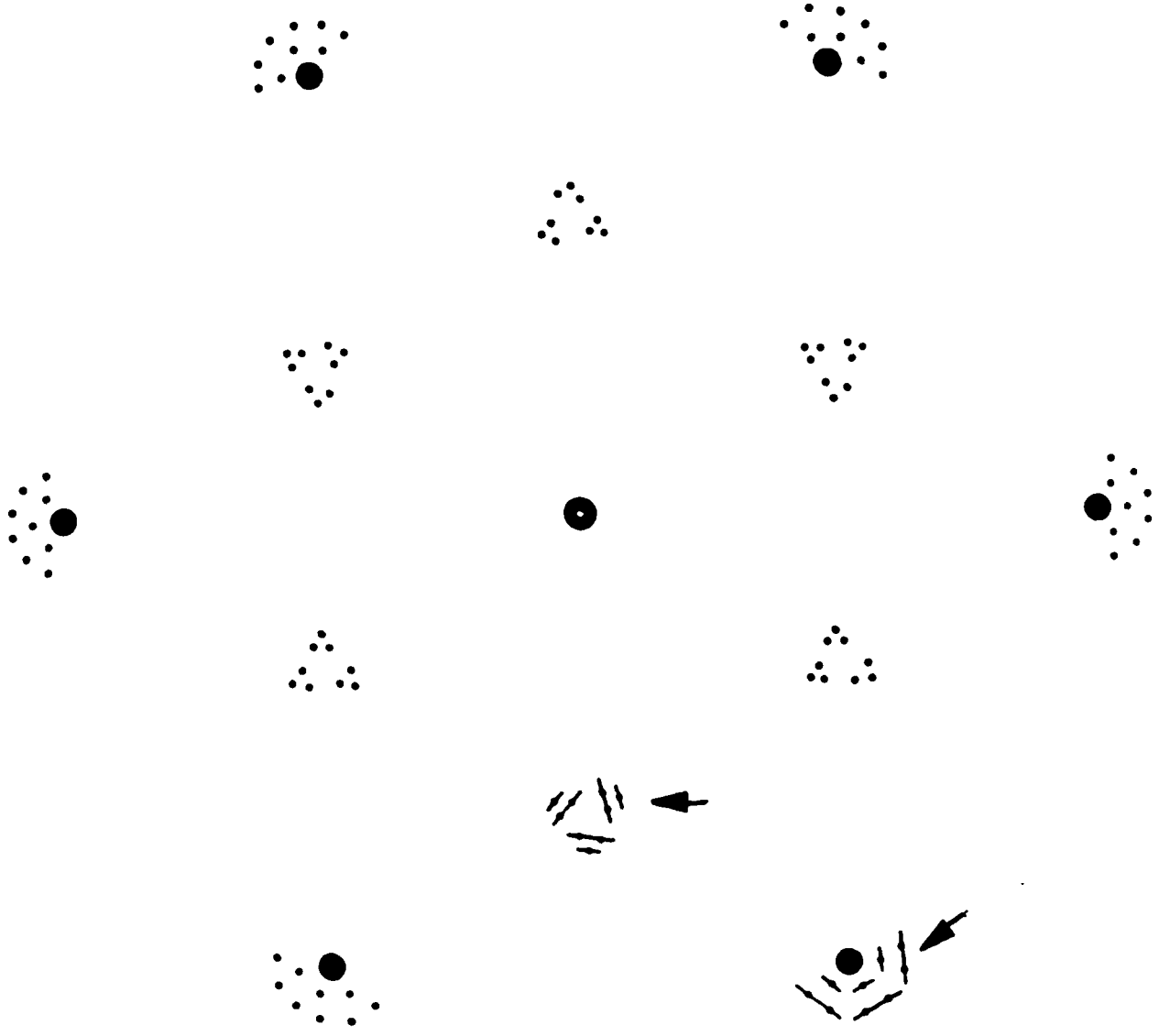


Figure III-20

The above pattern is generated when the pattern of Figure III-19 is generated about each of the six (220) Si reflections. The two arrows illustrate the strain effect on the pattern.

(1289H)

Each of the six strong (220) Si reflections can act as a primary beam for further diffraction in the PtSi layer. The total pattern is then generated by superimposing the original pattern around each strong Si (220) reflection. Figure III-20 shows the total pattern. Not all possible double diffraction reflections are shown, e.g., the ones forming the sidebands around the central spot. If strain occurs in the PtSi films so that lattice bending occurs, the PtSi reflections can be streaked. I have indicated the possibilities of this streaking in two locations shown in Figure III-20. Note that the diffraction pattern is now exactly generated (except for some doubly diffracted reflections not indicated).

The latest TEM studies were performed on 20A PtSi films. These films showed a good surface coverage and a high degree of epitaxy. Figure III-21 shows planar TEM pictures of 20A and 60A PtSi films on <111> Si formed at 425°C for six hours.

These are dark field images using a (220) Si reflection and the two (301) PtSi and one (002) PtSi reflections shown at position 2 of diffraction pattern in Figure III-22C. The Moire fringes are formed by interference of the PtSi reflections with the (220) Si as discussed previously. Since the 20A films are very thin, the contrast is not as good as in the 60A film since the intensity of the silicide reflection is weaker.

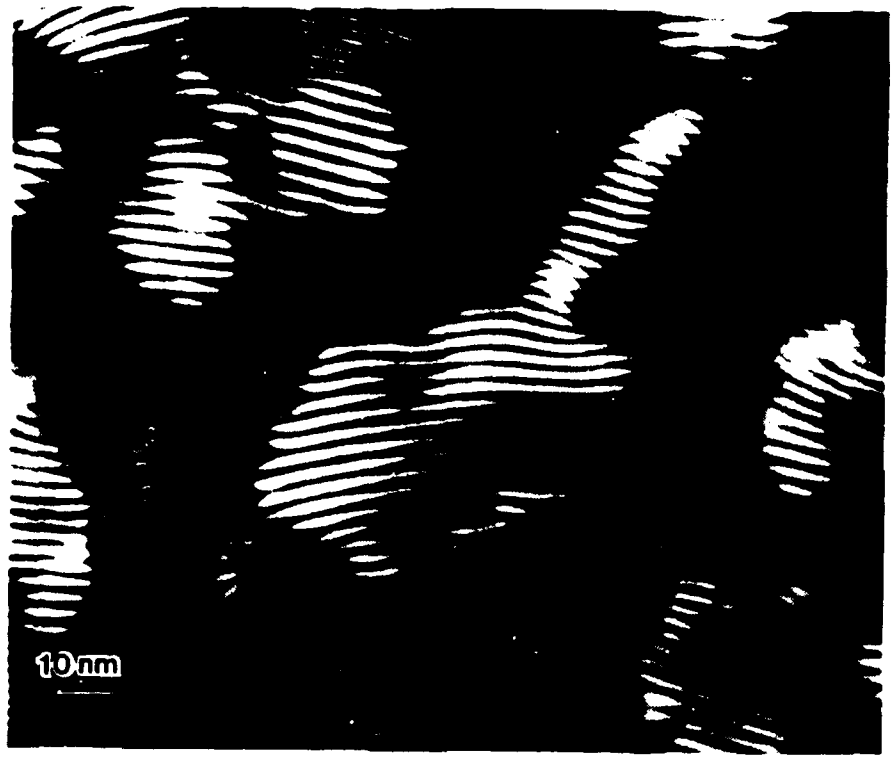
Note that the overall coverage of the 20A film is very good - comparable to that of the 60A film. However, the three variants are less distinct. The brighter areas (bright fringes) are again composed of regions which have one variant. The "domains" are smaller in the 20A film then in the

60A film. In the 20A film the fringes do not appear to have as much angular spread as in the 60A film, and the fringe spacing among the three variants is not as distinct. Also, the domain boundaries are not as distinct. This result is consistent with the diffraction pattern which shows the reflections from the PtSi variants beginning to merge and therefore the distinction between the three variants is less obvious.

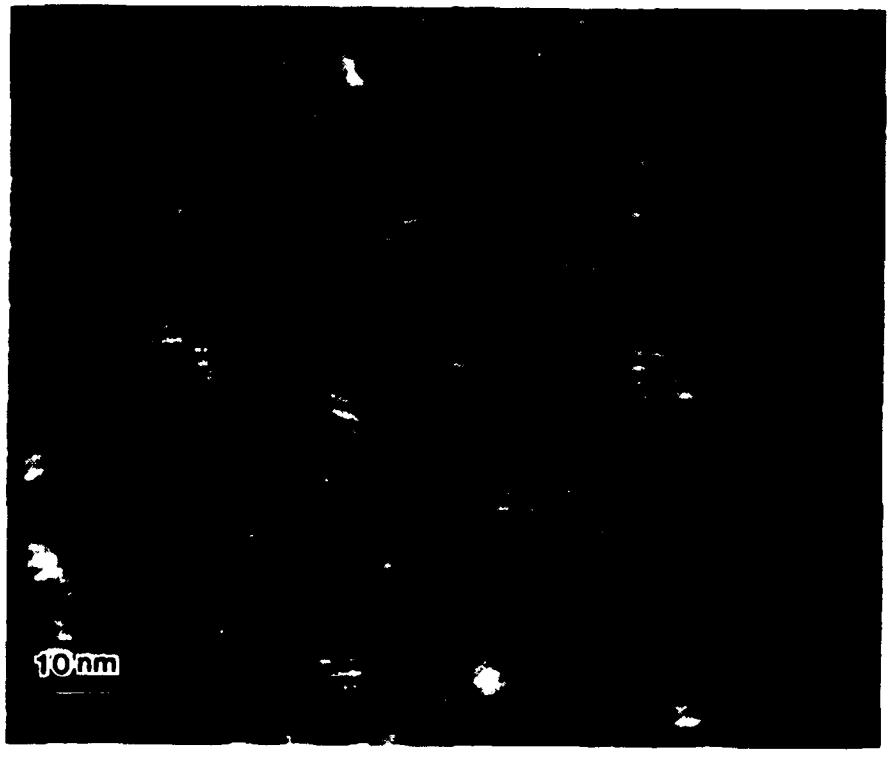
Electron diffraction patterns from planar specimens of PtSi on (111) Si are shown in Figure III-22. (A) shows pattern from 60A of PtSi reported on previously. 1 and 2 mark typical types of reflections. Those at position 1 are from 3 variants of silicide only. Those at position 2 are from silicide and a (220) Si type reflection.

C shows (at a larger scale) the disposition of reflections for an "ideal" pattern. The silicide reflections at position 1 form three groups. Each group is composed of three closely spared reflections - one from each variant. The small filled circles are primary reflections composing one group. The open circles are multiply diffracted reflections forming the other two groups. Note that the two (101) PtSi and one (200) PtSi reflection can be seen as a long and short streak respectively for the 60A films as shown in the higher magnification of position 1 at A.

The reflections at position 2 are composed of one (002) PtSi and two (301) PtSi as shown in C. (Multiply diffracted reflections are not shown). For the 60A film, all three of these can be resolved although the two (301) PtSi form a nearly continuous streak.



60Å PtSi/
111 Si

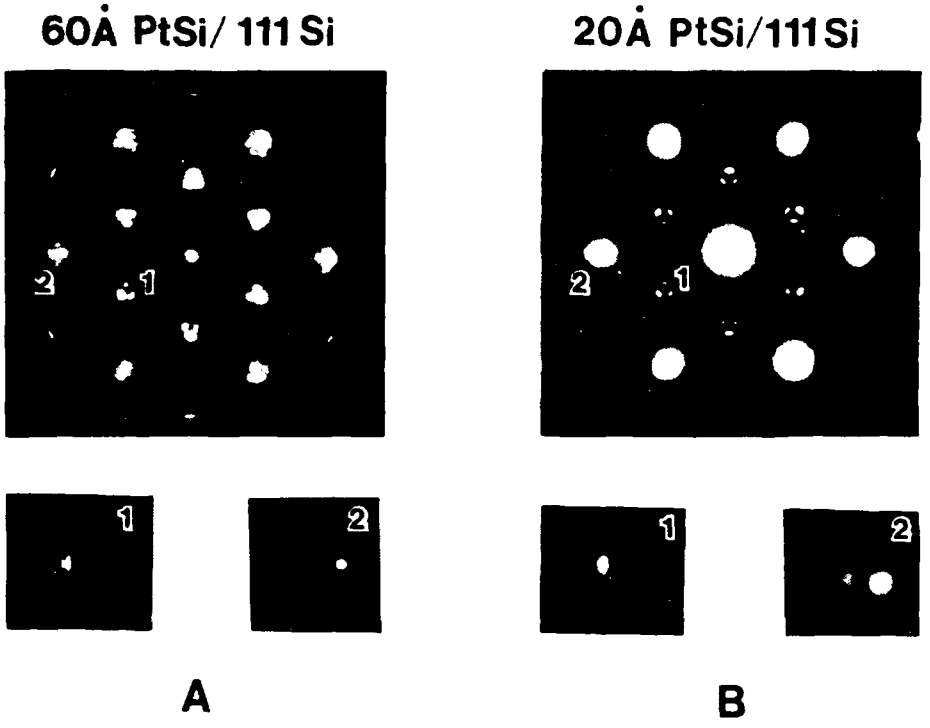


20Å PtSi/
111Si

Figure III-21 Moire Patterns of PtSi on (111) Si

The pattern for the 20A film is shown in B. Note that it is essentially the same pattern indicating the same PtSi orientation. However, the two (101) PtSi and one (200) PtSi reflections at position 1 have now merged into one reflection indicating a large amount of strain in the films. That is, the three variants are becoming indistinct. Likewise, the two (301) PtSi and one (200) PtSi reflections at position 2 are beginning to merge (the two (301) reflections appear as one) so that the films have not totally been constrained to the pseudohexagonal symmetry.

These pictures imply several significant results. First, from a crystallographic standpoint, a successful technology transfer with regard to pre-silicide clean and vacuum system parameters has occurred. Our uniform PtSi films on both (100) and (111) Si for PtSi thicknesses ranging from 20A to 80A PtSi indicate low partial pressure of O_2 ($\sim 10^{-8}$ torr) and low residual SiO_2 coverage on the Si surface. If more SiO_2 (~20A) were present on the surface, the PtSi film thickness would be much more non-uniform and there would exist areas devoid of PtSi formation. From this analysis, a conservative estimate is made of greater than 90% PtSi film coverage for both the 20A PtSi and 80A PtSi films. Secondly, on the (111) Si substrate, virtually all of the PtSi formed is oriented with respect to the Si, with increasing evidence of strain on the thinner (20A PtSi) films. There are three variant orientations, all having (020) PtSi parallel to (111) Si. The three variants occur because the (002) PtSi can align along either the (220) Si, (220) Si or (022) Si.



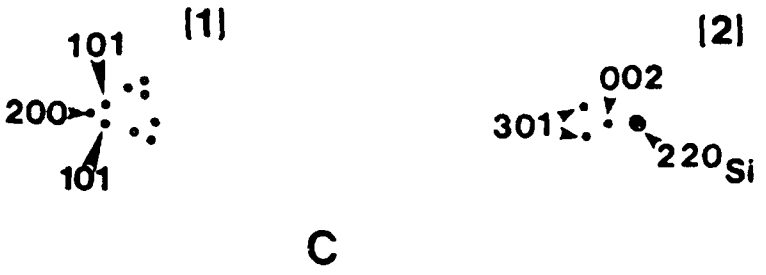


Figure III-22 - Diffraction Patterns on 60A and 20A PtSi Films on (111) Si

Thirdly, our analysis shows that the PtSi/Si interface is smoother for the films formed on (111) Si versus (100) Si. This was expected since the PtSi is more epitaxial on the (111) Si than on the (100) Si. Finally, we see larger grain sizes and more grain interconnections for the PtSi formed on the (111) Si as opposed to that formed on the (100) Si.

2. Process Variations

PtSi sensors were fabricated at the R&D Center and at ATL over the course of the program. The baseline process is described in the Interim Report and only the PtSi matrix will be discussed. The PtSi fabrication variations included:

(1) Si substrate orientations of (100) Si and (111) Si.

(2) PtSi thicknesses from 10A to 80A.

(3) PtSi anneals of ~400°C to 650°C.

(4) Use of two deposition systems [one of MBE quality ($\sim 10^{-11}$ torr) and one of HV quality ($\sim 10^{-8}$ torr)], both being non-oil-based pumped.

The general direction of the process changes were to thinner diodes, lower anneal temperatures and lower evaporation pressures. Reducing the films thickness generally increases the infrared response by reducing the barrier value and increasing the C_1 Fowler coefficient. Lower anneal temperatures and lower evaporations pressures have reduced the reverse bias diode leakage, but all diodes tested show a soft reverse bias breakdown. The characteristics and pressures of the HV evaporator located at ATL have been discussed in the

Interim Report. The majority of the PtSi films have been fabricated using this HV system. The MBE system located at the R&D Center has been used in the later stages of the program. The discussion which follows describes the UHV system, its analysis equipment and results which have been observed.

3. MBE Introduction

The MBE system consists of four interconnected chambers shown schematically in Figure III-23. Three of the chambers were designed and fabricated by ISA/Riber, a well-known manufacturer of conventional semiconductor MBE equipment. The chambers incorporate standard UHV technology, being constructed completely of stainless steel, with copper-gasketed flanges and an absolute minimum of elastomer seals. The chambers are pumped by ion pumps, cryopumps, and titanium sublimation pumps; and the introduction chamber is roughed by oil-free absorption pumps. The deposition system uses molybdenum substrate mounting blocks, on which wafers up to two inches in diameter can be mounted, and then inserted onto the stages of a manipulated holder in the introduction chamber. After initial thermal degassing and/or low energy ion surface cleaning, the blocks are moved to other chambers by the use of magnetically coupled transfer rods. Each chamber has a manipulator with two stages, one heated and one unheated. Samples may be heated as high as 1200 or 1250°C in the introduction and deposition chambers. The complement of equipment in each chamber is listed in Figure III-23.

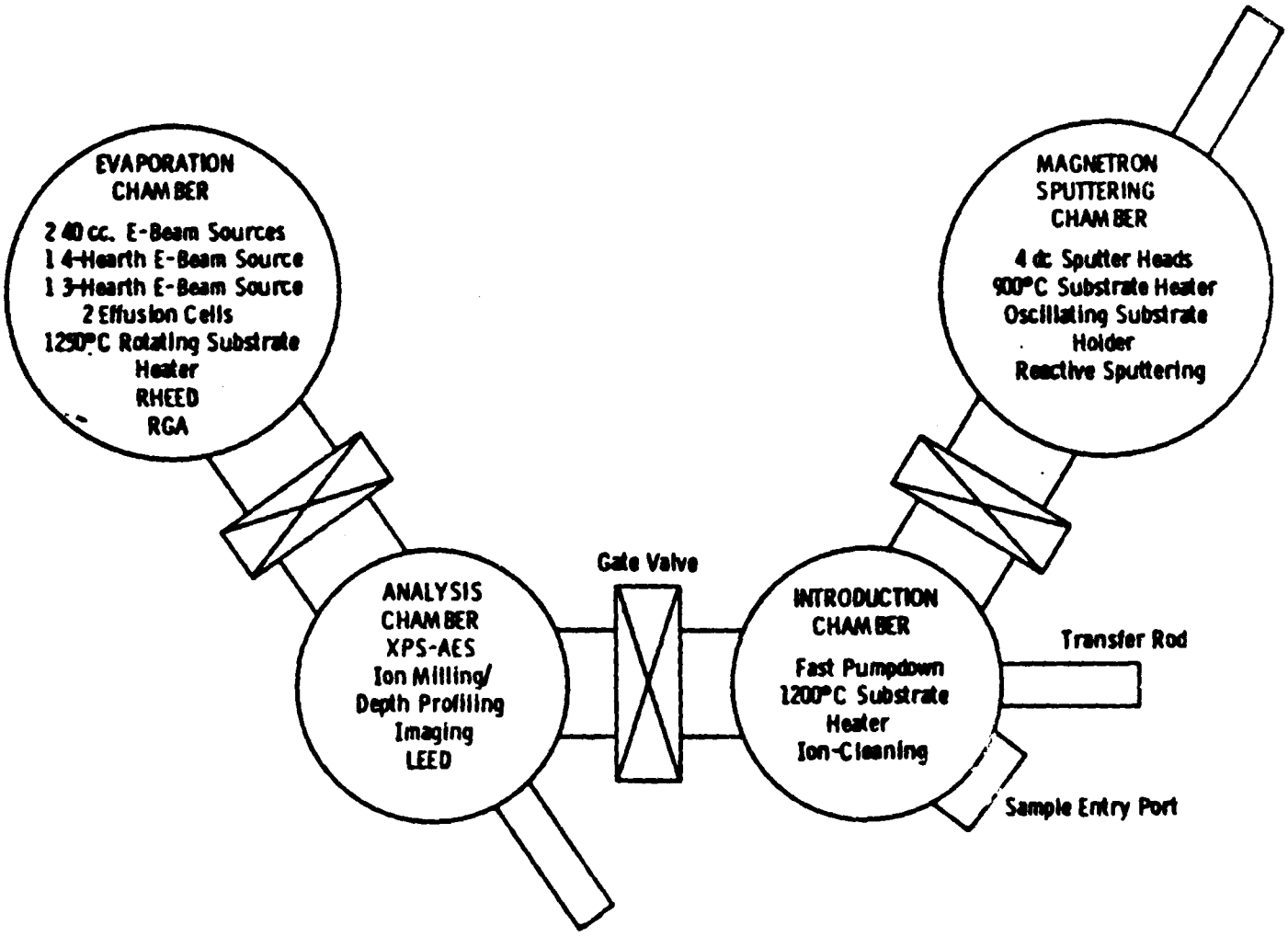


Figure III-23

(1289H)

The key feature of the system is the large deposition chamber, oriented for vertical deposition so that e-beam heated sources can be used, and with its inner surfaces, shielded by double-walled, liquid nitrogen filled cryoshrouds to preclude exposure to the intense radiant heat from the e-beam sources. These cooled surfaces minimize the heat-induced outgassing or desorption of surface contaminants during film deposition, and thus allow the maintenance of deposition vacuum in the low-10^{-10} or even mid-10^{-11} torr range, depending in part on whether the large or the small e-guns are being used, on the species being deposited, and on the length and rate of deposition. The usual base pressure in the deposition chamber before deposition, with the cryopanels cold, is between 2 and $5x10^{-11}$ torr. Though the monolayer time (the time for a monolayer of contamination to form, assuming unity sticking coefficient) at 10^{-10} torr is six hours, contamination with orders of magnitude less than a monolayer may be sufficient to interfere with silicide formation, particularly if epitaxial silicides are desired, so the best possible vacuum is desirable.

The available elaborate deposition rate monitoring equipment can be used for rate control of the sources, but for the silicide work it sufficed to measure the total deposited Pt thickness using a quartz crystal thickness monitor located close to the substrate and adjusted to have a resolution of 0.05 Angstrom of Pt. The RHEED gun and screen are so arranged that the surface of the sample can be monitored during deposition, if desired. In practice, with refractory metal sources which give off so much light as to wash out the pattern on the RHEED screen, and with the desirability of sample rotation during deposition to achieve the best possible thickness uniformity, the usual procedure is to observe the substrate and film surfaces with RHEED just before and just after film deposition.

The analysis chamber has both Auger electron spectrospcopy (AES) and x-ray photoemission spectroscopy (XPS) available. The primary advantage of AES over XPS is the possibility of focusing the electron beam of AES to analyze a small area. However, for analysis of freshly deposited films which cover large areas, XPS is preferred because the chemical shifts are more easily interpreted. XPS analysis was employed for the silicide work. A new reverse view low energy electron diffraction (LEED) instrument was recently installed in the analysis chamber, allowing observation of diffraction patterns related to the geometrical arrangement of atoms in the topmost one or two atomic layers of substrate or film. The reverse view feature allows observation of any part of even the largest substrates, without obstruction of the view of the pattern of the fluorescent screen.

A typical run begins with chemical cleaning of the wafer to remove particular, metallic, and organic surface contaminants, followed by treatment with HF to remove oxide from those areas of the silicon which are not purposely oxide masked. To prevent reoxidation, the wafer is not rinsed in pure water after the HF treatment, but is immersed in very diluted HF/water and then blown dry. It is then quickly mounted by loosely fitting clamps to a molybdenum sample mounting block and inserted into the introduction chamber. The introduction chamber is pumped into the low-10^{-8} torr and is capable of 300°C bake, depending on what characteristics of the substrate surface are of interest. The sample then is transferred to the analysis chamber and baseline XPS analysis may be performed to ascertain the amount of oxide and carbon contamination. Next, in the deposition chamber, RHEED (Reflection High Energy Electron Diffraction) shows the initial substrate surface condition (supplemented by LEED in the case of later runs). The block may be strongly heated to 1000 or 1100°C or in some cases even higher, reaching these

temperatures in about 10 minutes. Temperatures given in this report are block temperatures, not necessarily actual substrate temperatures, which may be considerably lower. Actual calibration of wafer surface temperature to block temperature has not been carried out. It is sufficient that the temperature effects be reproducible. Residual gas analysis (RGA) in the deposition chamber shows what absorbed contaminants are outgassed from the block and substrate. LEED, RHEED and XPS are used to determine surface condition and amount of oxygen and carbon contamination remaining, with further annealing iterations performed as required to produce the desired surface cleanliness. Then follows the deposition of Pt to the desired thickness, usually with the block at low temperature (less than 100°C in some cases sub-room temperature, because of the surrounding cryoshrouds). The substrate is rotated at about 23 rpm during deposition to improve thickness uniformity, and the rate of deposition is adjusted manually from approximately 0.1 Angstrom per second for the thinner films, up to the range of 0.5 Angstrom per second for the thicker deposits. Vacuum levels are read just before and just after deposition (ion gauges being inoperative or giving erroneous readings during deposition due to stray electrons from the e-gun sources). After deposition and appropriate diffraction and XPS analysis, the Pt layer is reacted thermally by heating in the deposition chamber, usually while being monitored by RHFED. Details of analysis procedure and thermal reaction schedules varied from run to run, depending upon the purpose of the run. After these procedures are completed, the block is removed from the system via the introduction chamber. No special care has been taken to minimize or characterize post-removal surface atmosphere interactions.

4. Chemical Cleaning Procedures for Silicon Wafers

The cleaning procedure roughly follows that given by Christou et al[12]. The wafer is first cleaned by "spin scrub" to remove particulate contamination, and then subjected to a sequence which has an ammonia based dip to remove carbon and metallic ions, and an HCl/peroxide dip to reoxidize the Si surface. The HF dip is necessary to thin the regrown oxide and supposedly to make it more porous, so that low temperature desorption is accomplished more readily. We have found in later runs that omission of any final deionized water rinse - and instead rinsing in very dilute HF/wafer - seems to facilitate the thermal desorption of the oxide, as does immediate insertion of the wafer into the vacuum system after its removal from the HF.

For runs R86-28 and R86-35, a different cleaning procedure was used prior to the HF dip, in order to duplicate the entire silicide formation sequence as used by RADC.

5. Mounting and Temperature Measurement of the Wafers

In the earlier runs before run R85-72, the 2" diameter wafers had to be cut (by scribing and breaking) to a 1 1/4" width to accommodate an already available clamping arrangement in place on the Riber molybdenum sample blocks. For Run R85-64 and later, the clamps were modified so as to capture the wafer but not to press it tightly against the block. In fact, in the deposition position, in which the wafer surface faces downward, there would be a gap of approximately 0.020" between the wafer and the block. Temperature uniformity was visibly improved. A new block was placed in service, starting with Run R85-72, with peripherally located clamp screws which allow mounting of an uncut 2" wafer, still held loosely.

As is always the case, there is an unknown differential in temperature between the thermocouple, which is inserted into a surrounding well in the back of the mounting block, and the actual temperature at the surface of the substrate. The thermocouple cannot make actual contact with the block, because the block is rotated during depositions, and the wafer itself appears to be much lower in temperature than the block at the 1000 or 1100°C nominal block temperatures used for oxide desorption annealing. The actual silicon surface temperature may also be affected by the radiative environment, as during annealing it is surrounded in the deposition chamber by liquid nitrogen cooled surfaces. This arrangement is to be preferred to some sort of radiation shield, effectively an oven, which might be placed around the wafer to help bring it to block temperature, because such an oven would also confine desorption products to the vicinity of the wafer, degrading the vacuum locally.

In any event, the actual temperature differential is unimportant for the present series of runs, so long as it is reproducible. For transfer of the silicide technology to other equipment, the actual wafer temperatures will have to be determined.

6. Annealing and Surface Reconstruction of the Silicon

Because the purpose of this work is to form the thinnest, highest purity silicide layer with the best possible planar abrupt silicon-silicide interface, purity and surface quality considerations are paramount. Impurity concentrations in the initial metal film or at the Pt-Si interface cause macroscopically non-planar PtSi-Si interfaces and PtSi surfaces[13]. Oxygen, especially, is deleterious in its effects on the silicide formation process, by causing a disruption of the normal phase growth sequence[14] and

a decrease of growth rate by up to a factor of twenty[15,18]. Therefore high purity must be deposited in the purest ambient conditions, i.e., the best possible vacuum, and the surface receiving the deposit must be as free as possible of other atomic species, particularly oxygen. Hence, a large fraction of the effort goes into cleaning the silicon surface. The initial cleaning and HF dip have been described. The cleaning continues by in-situ annealing in the best possible vacuum to remove oxygen and carbon.

The ultimate clean silicon surface is generally considered to be indicated by a 7x7 reconstruction as seen by RHEED and/or LEED. But ever since a reconstructed surface was first seen on an "atomically clean" surface thirty years ago[17], there has been controversy about what impurities, if any, may reside at (or beneath) particular sites on the reconstructed surface. Certain reconstructions are attributable to contamination, such as Si (111) $\sqrt{19}$x$\sqrt{19}$ with nickel[18,19] or carbon[20] and there are recent studies using scanning tunnel microscopy which attempt to connect Si (111)-7x7 characteristic defect sites with impurities such as surface segregated boron in p-doped Si[21]. This would imply surface considerations of boron several orders of magnitude higher than equivalent bulk dopant levels. Effects of such high boron concentrations on silicide formation have not been directly studied. Thus what has been deemed to be the cleanest possible surface on (111) silicon may not be so at all. To quote the 1983 review article by A. Kahn on semiconductor surface structures[22] ". . . the (7x7) reconstruction of Si (111) remains a wide open issue which will undoubtedly generate much interest during the next few years." While we wait for the issue to be settled, we have adopted a working criterion that the 7x7 reconstruction represents the cleanest surface condition. A $\sqrt{3}$x$\sqrt{3}$

reconstruction is also seen, but is associated with lower annealing temperatures and higher oxygen levels as seen by XPS. The $\sqrt{3}x\sqrt{3}$ can be transformed to 7x7 by longer or higher temperature annealing. The $\sqrt{3}x\sqrt{3}$ represents a shorter periodic structure than the 7x7, so there are fewer periodic sites in the 7x7 to be associated with impurities (if they are associated). Recently a 5x5 reconstruction has been observed, which probably is intermediate in surface contamination between the $\sqrt{3}x\sqrt{3}$ and the 7x7.

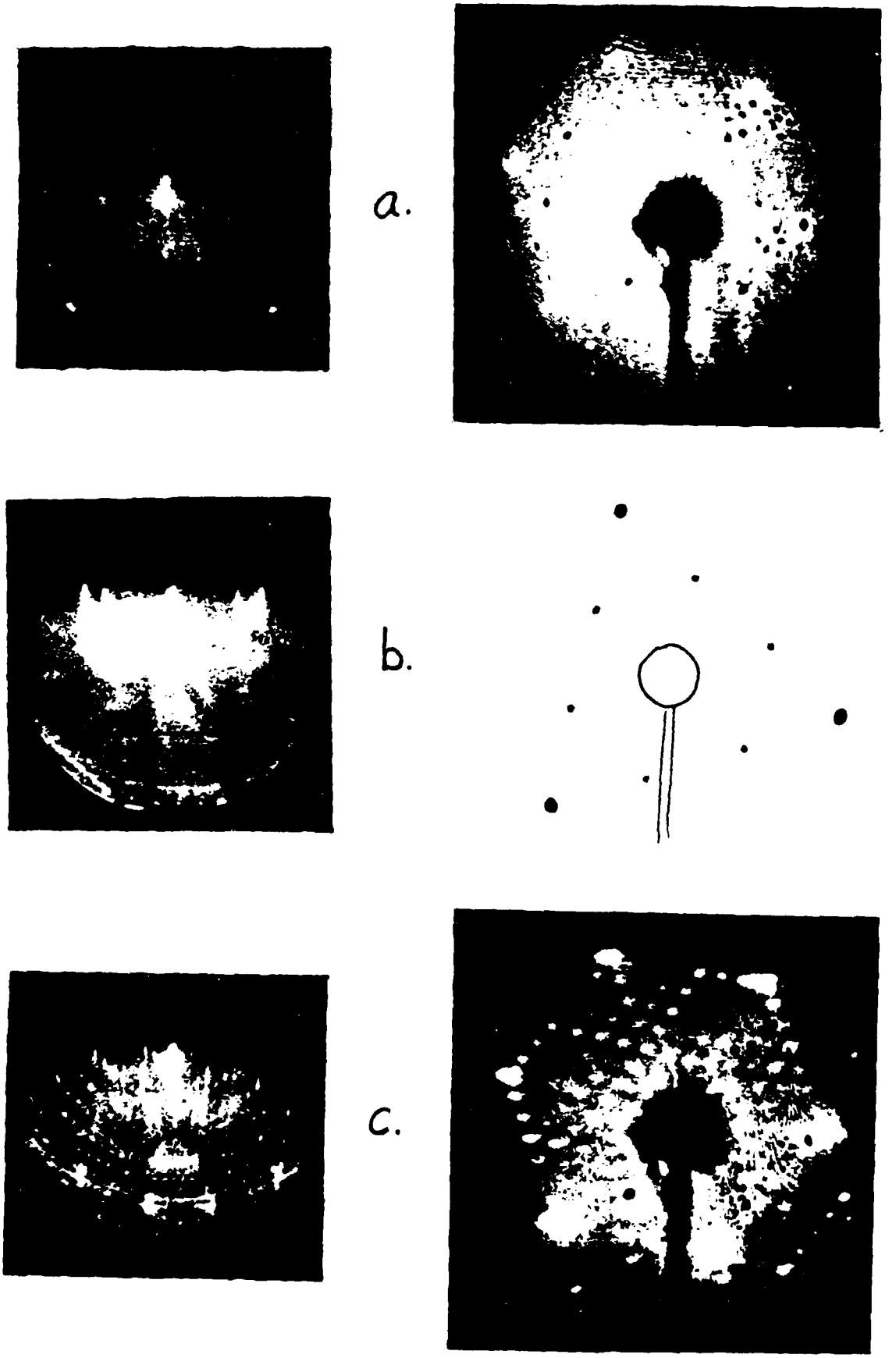
Even if there are no impurities at periodic reconstruction sites on the surface, the sites may still have some effect on silicide layer formation, especially when the layer is only a few Angstroms thick. Such effects are report[23] for Ge epitaxially grown on Si (100)-2x1 and on Si(111)-7x7. On the other hand, the interdiffusion of the Pt and Si at the interface prior to the epitaxial formation may minimize or eliminate such surface defect state effects.

Concerning the actual achievement of reconstructed silicon surfaces, the experience so far is that an indicated annealing temperature of 1000°C (of the mounting block, not necessarily the wafer) will produce 7x7 if the wafer has been loaded quickly after an adequately strong HF dip and if the resident time in the vacuum system is shorter than a few hours. For longer dwell times, a 1000°C anneal will only produce $\sqrt{3}x\sqrt{3}$, but this may then be transformed to 7x7 by an 1100°C anneal. For very long dwell times (days) even 1100°C will only produce $\sqrt{3}x\sqrt{3}$, (as for R85-71). A good 7x7 will degenerate if allowed to reside for 20 to 30 hours in the vacuum system, and cannot be regenerated by subsequent annealing (R85-40). This degeneration may be correlated with having the surface facing the ionization gauge for long periods of time.

Figure III-24 shows RHEED (left) and LEED (right) pictures for unreconstructed, √3x√3, and 7x7 reconstructions. The center LEED sketch was made before a camera was obtained for the LEED instrument.

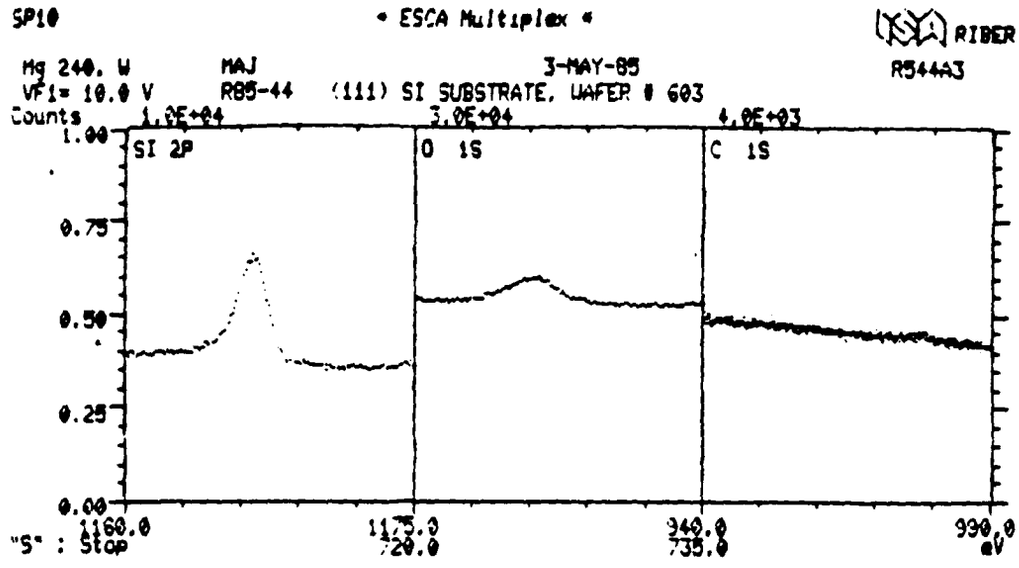
The upper left RHEED picture in Figure III-24 of Run R85-40, demonstrates what has happened to a nicely reconstructed 7x7 surface which was allowed to sit in the vacuum system (after one day the 7x7 pattern had disappeared and the surface was 1x1). Reannealing after sitting two days produced a √3x√3 reconstruction which does not show up particularly well in this <10$\underline{1}$> azimuth, but was definitely obtained after the reanneal, the RHEED photo of the <$\underline{2}$11> azimuth being identical to that of Run R85-32, which is shown in Figure III-24b, left.

XPS analysis provides additional information on identity of impurity species. Figure III-25 shows raw XPS data from the (bare silicon) wafer identification number area of the wafer of Run R85-44, after (a) degassing at 330°C, (b) first 1000°C anneal, and (c) second 1000°C anneal. The small carbon 1S peak completely disappears after the first anneal. The reduction of oxygen by the annealing can be easily followed by observation of the O 1S peak. The O 1S data from these traces are shown expanded vertically and superimposed in the top graph of Figure III-26. After the second anneal, the oxygen peak is just about gone, and a 7x7 reconstruction was seen; Figure III-24c, left, is a RHEED picture from this run just after the first anneal. This is perplexing, because even though the surface is already showing 7x7 reconstruction after the first anneal, there is still oxygen visible by XPS which can be reduced by further annealing. This may be explainable by the fact that RHEED is not easy to localize to any particular small part of the wafer, so exact coincidence of the XPS- and RHEED-analyzed areas is not to be



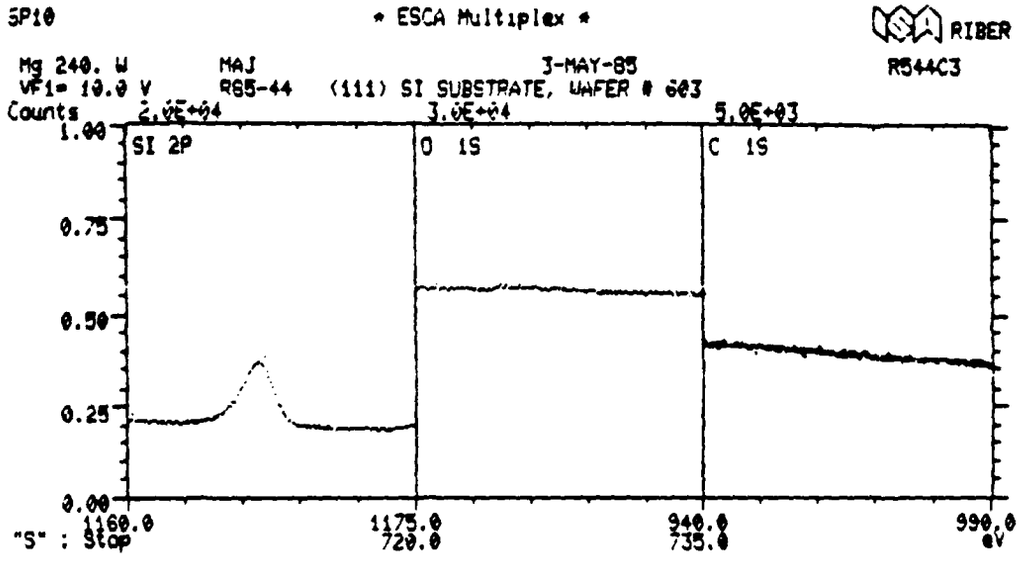
⟨111⟩ Si reconstructions by RHEED (left) and LEED (right). A. 1x1 reconstruction B. $\sqrt{3} \times \sqrt{3}$ C. 7x7

Figure III-24

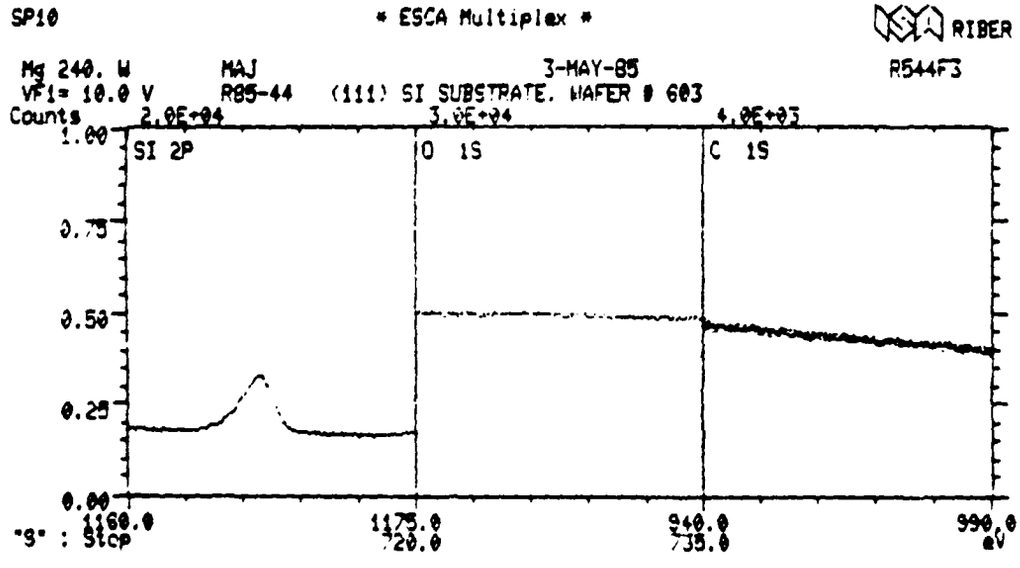


XPS of wafer in run R85-44

a. After 330° C degas



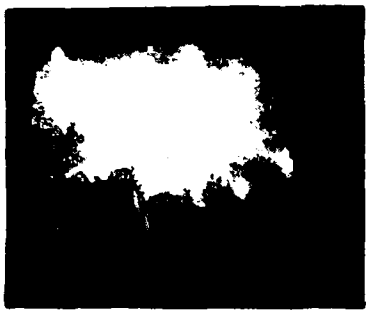
b. After 1st 1000 C anneal



c. After 2nd 1000 C anneal

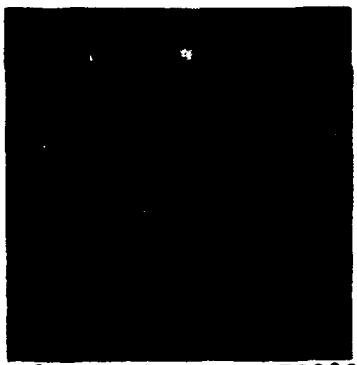
Figure III-25

PLATINUM SILICIDE FORMATION

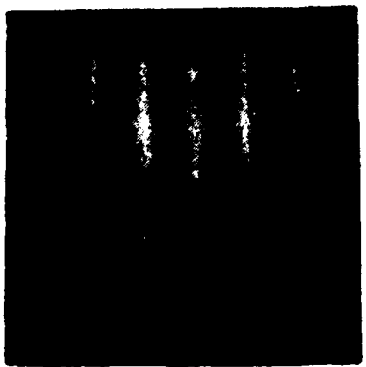


(111) Si, ANNEALED 1000°C

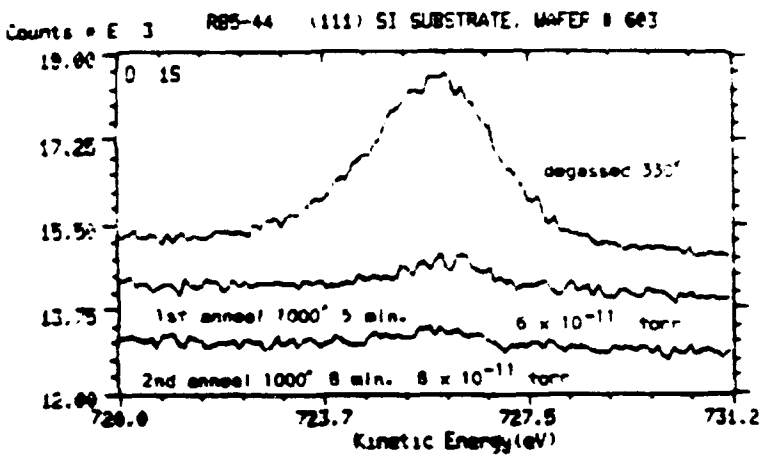
50Å Pt, DEPOSITED 30°C



20Å Pt, ANNEALED 300°C



20Å Pt, ANNEALED 405°C
(460°C ANNEAL IS IDENTICAL)



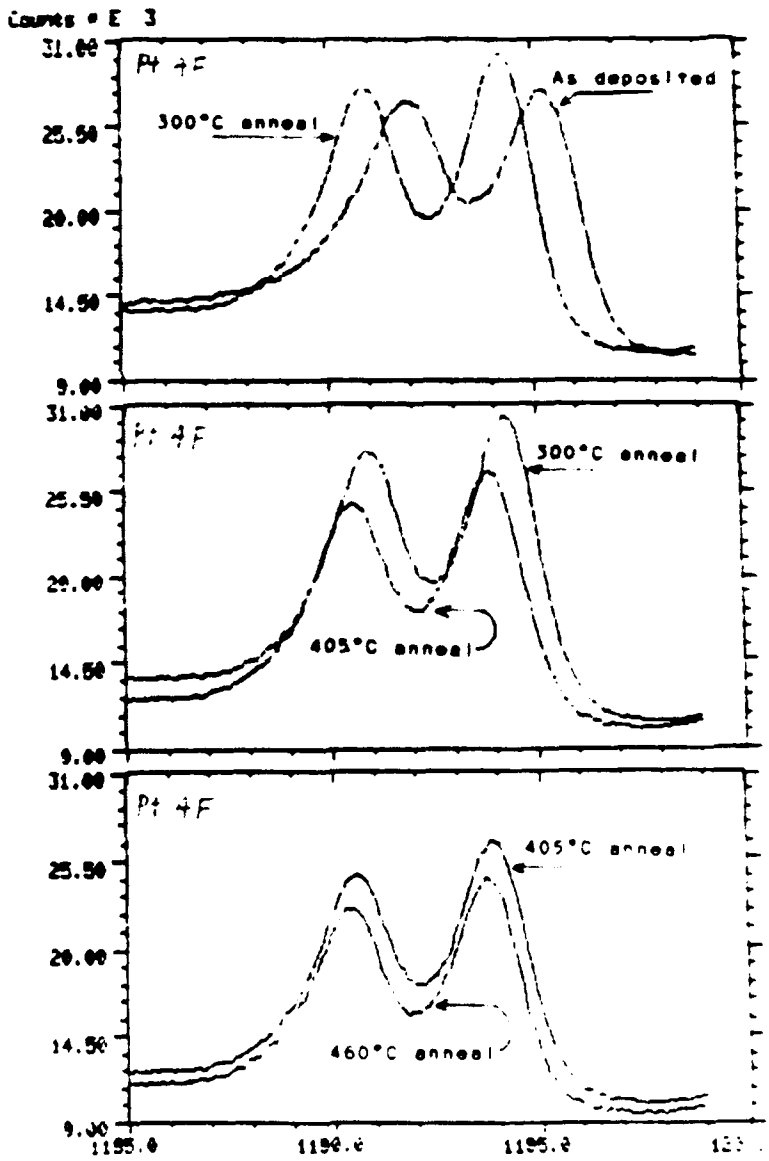


Figure III-26

expected. The XPS-analyzed area, being at the edge of the wafer and therefore reaching slightly lower peak annealing temperatures, may retain oxygen longer than the center part of the wafer, the area from which the RHEED pattern is generated. Disappearance of oxygen can also be seen by observing the Si 2P peak (a peak due to SiO_2 seen adjacent to the main Si peak). This satellite peak diminishes as the oxide is removed. However, as this satellite peak sits on the shoulder of the main Si peak, its decrease is not as definite and thus is not as informative as the disappearance of the O 1S peak. In fact, the SiO_2 peak is all but invisible even in Figure III-25 (a) before any annealing. For comparison, an XPS analysis of an oxide bar masked area is shown in Figure III-27, in which the SiO_2 peak is larger than the Si peak, and the O 1S peak is very strong.

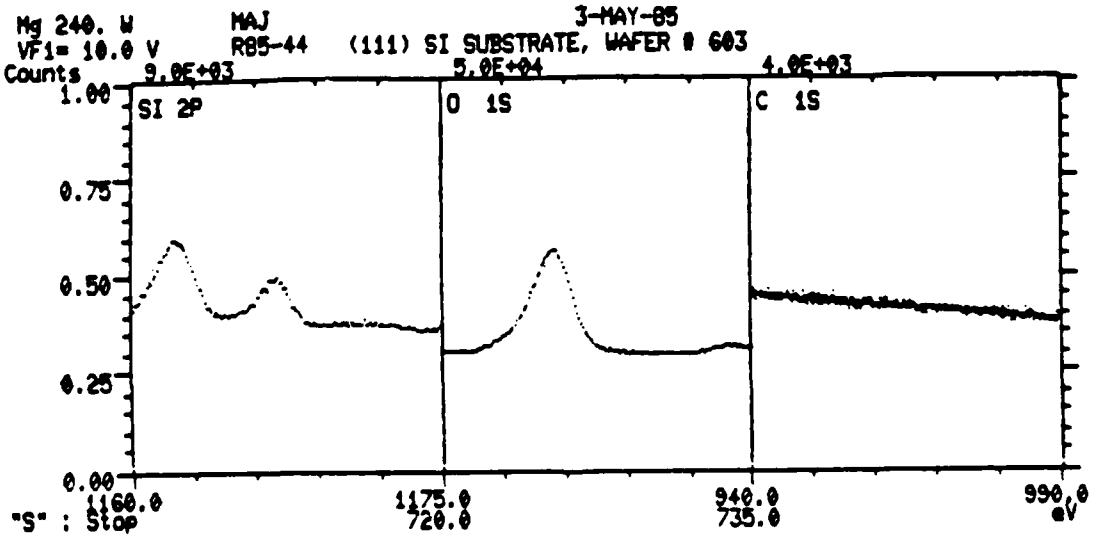


Figure III-27

7. Diffusion and PtSi Formation as Seen by RHEED and XPS

The RHEED observations of the thicker layers of Pt deposited on clean Si surfaces and then thermally reacted can be nicely correlated with kinetic energy shifts of the Pt 4F photoelectron peak. The second RHEED picture in Figure III-26 is of a 50 Angstrom as deposited Pt film (Run R85-35). The broken ring pattern is characteristic of a polycrystalline film with some texturing or non-random orientation of the grains. The third RHEED picture (Run R85-40) shows the typical alteration of the Pt structure with a 300°C anneal. Only a very faint and broad single ring can be discerned, along with the central specular reflection of the incident electron beam. This indicates that the surface layer is disordered, either amorphous or very fine-grained polycrystalline and would be consistent with the diffusion of the Pt into the Si without forming any particular stoichiometric Pt-Si phase. In the second graph of Figure III-26 the Pt 4F photoelectron peak shows a 1.0 eV energy shift to a higher binding energy after the 300°C reaction. Apparently all of the Pt reacted, because the Pt 4F doublet had no additional splitting. For thinner layers of Pt, or for runs when the Pt was deposited on substrates above 20°C, this disordered RHEED pattern and associated XPS peak shift appear without any annealing.

Further higher temperature annealing is necessary to form the PtSi phase. This annealing is usually carried out while monitoring the surface structure with RHEED. The bottom RHEED picture shows the fully developed PtSi pattern (Run R85-40). Higher temperature annealing has no further effect on the pattern, with the exception of increasing the spottiness of the streaks. For thinner Pt films, such as R85-70 (10 Angstroms of Pt), the pattern becomes

fainter, with the half-order streaks disappearing. For the 5 Angstrom Pt film of Run R85-12, only the three intense streaks closest to the center of the pattern remain, and they are faint, broad, and fuzzy. The third graph of Figure III-26 shows the further Pt 4F peak shift to a total of 1.35 eV from the as-deposited position. The fourth graph for the 460°C anneal shows a slight additional shift to 1.50 eV from the initial as-deposited position. Table III-2 summarizes the runs performed on the MBE machine.

8. IR Response

Infrared photoresponse measurements (from 2.0μ to 5.5μ) were made on PtSi diodes fabricated from the five wafers fabricated at ATL and at the R&D Center. These measurements were performed on two size diodes, 1000μ x 1000μ and 200μ x 200μ. Initially, the temperature of operation of the diodes was T = 35K, but later changed to T = 77K. Subsequently, 77K was used for majority of the IR response measurements. No change in IR response was observed upon changing the operating temperature. The photoresponse flux measurements employed a glowbar, a set of calibrated narrow band pass filters, lock-in amplifier and calibrated thermopile. It was determined that low energy light leakage was a problem for the 2.0μ, 2.5μ and 2.8μ filters and that a ~1μ - 3μ band pass filter operated in series with the narrow band pass filters was required and used. A reverse bias of 3 to 6 volts with a ~1000 Hz chopping frequency were used on the Schottky diodes for the photoresponse measurements. On these diodes, there was no change in the photoresponse signal when either the bias was changed (from 1 volt to 20 volts reverse bias) or if the chopping frequency was changed (from 100 Hz to 10 kHz).

IV. Summary of MBE PtSi Runs

R85-32	√3x√3, no Pt deposited
R85-35	√3x√3, 50A Pt, 460°C, sharp PtSi RHEED
R85-40	√3x√3, 20A Pt, ?°C, sharp PtSi RHEED
R85-44	7x7, 15A Pt, 417°C, sharp PtSi RHEED (patterned wafer)
R85-64	Run aborted, stubborn oxide (patterned wafer)
R85-68	1x1, 40A Pt, 460°C, usual RHEED, fuzzy hex LEED (patterned wafer)
R85-70	7x7, 10A Pt, 606°C, fuzzy RHEED, fuzzy hex LEED (patterned wafer)
R85-71	√3x√3, 10A Pt on 400°C Si, 615°C, med sharp RHEED, complex hex LEED, sharp spots (patterned wafer)
R85-72	7x7, 5A Pt, 560°C, faint RHEED, Triang LEED (patterned wafer)
R85-73	7x7 LEED, 1x1 RHEED, 10A Pt, 413°C, fuzzy RHEED, fuzzy hex LEED (patterned wafer)
R86-28	A100 wafer <100>, RCA clean, 230°C degas only, no RHEED, 5A Pt, 450°C 30 min (patterned wafer)
R86-35	B100 wafer, <100>, RCA clean, 1100°C anneal, 5A Pt, 450°C, 5 min (patterned wafer)
R86-49	A111 wafer, <111>, C3B clean, 1045°C anneal, 5x5 recon, 5A Pt, spotty RHEED, 477°C, 1 min, fuzzy RHEED patterned wafer
R86-50	B111 wafer, <111>, C3B clean, 1050°C anneal, 1x1 recon, 5A Pt, 480°C, sharp RHEED, hex LEED patterned wafer

(1289H)

The response data represents an averaged value obtained from data of two to four diodes. This was done to average out the data scatter. Since each particular average was performed on diodes located on the same wafer, but placed at slightly different positions in the dewar, the varying response mainly reflects the non uniformities in the IR source. Moving the optical axis over the range of sensor sites yielded a ~10% variation in signal. This gave an over estimate of the spatial non-uniformity of the infrared illumination. The un average diode data is presented in the Appendix. As discussed in the Seventh Quarterly Report, neighboring diodes were reverse biased to eliminate unwanted response signal. This significantly reduced the response variation versus diode size problem observed early in the program.

Figure III 28 represents the best response from all the diodes tested. [illegible] response dependence on diode size which has not completely been eliminated by biasing neighboring diodes but is not deemed [illegible]. A more accurate measure of C_1 should be from the larger diodes [illegible] smaller diodes has less influence on the response of a larger neighboring diode than vice versa. A definite barrier shift from ~.3eV to [illegible] evident upon decreasing the PtSi thickness from 20A to 10A. C_1 [illegible] both thicknesses are ~17-19% for the 1mm x 1mm diodes.

[illegible] 29 presents response data vs PtSi thickness variations. An already noted barrier decrease and increase in C_1 value occurs upon decreasing the PtSi thickness. The 40A and 80A PtSi films were fabricated at [illegible] while the thinner films were deposited at the R&D center using the MBE system. Actual [illegible] thickness may vary between the two

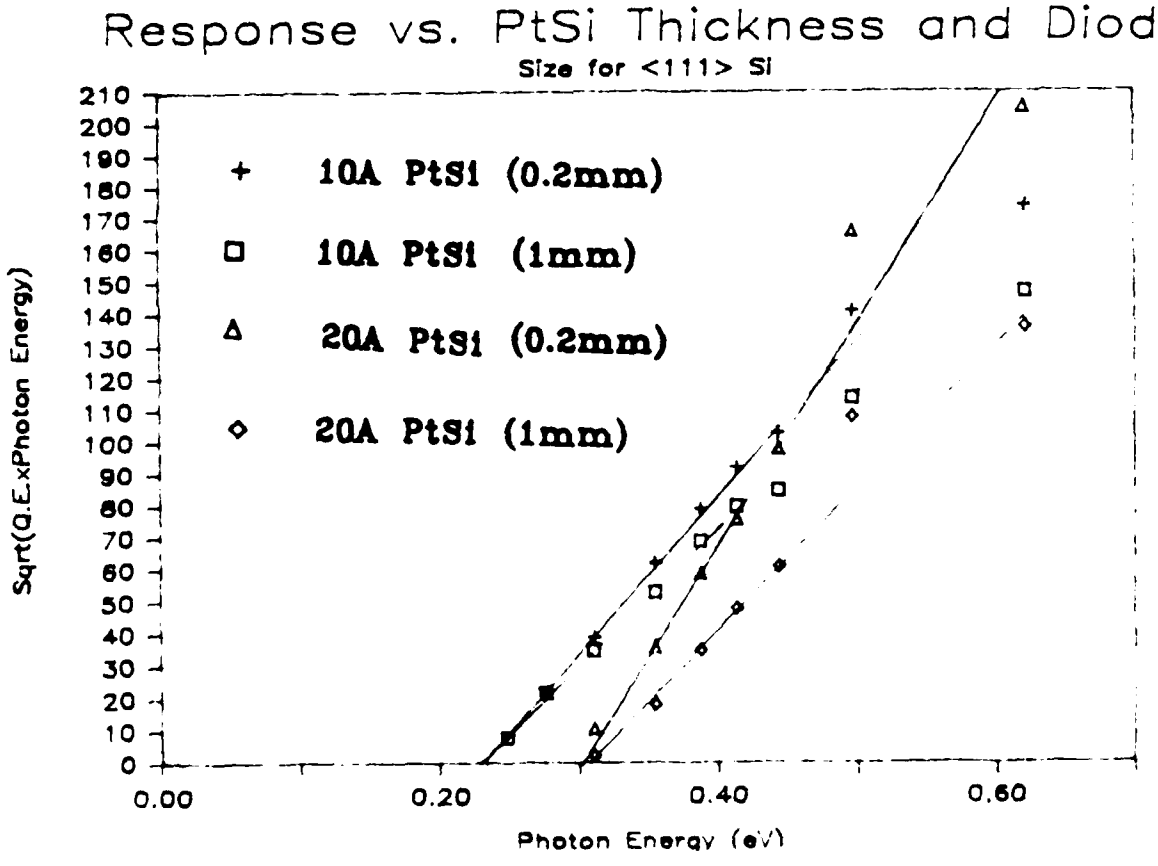


Figure III-28 - MBE PtSi Samples Formed at 560°C and 600°C Anneal

(1289H)

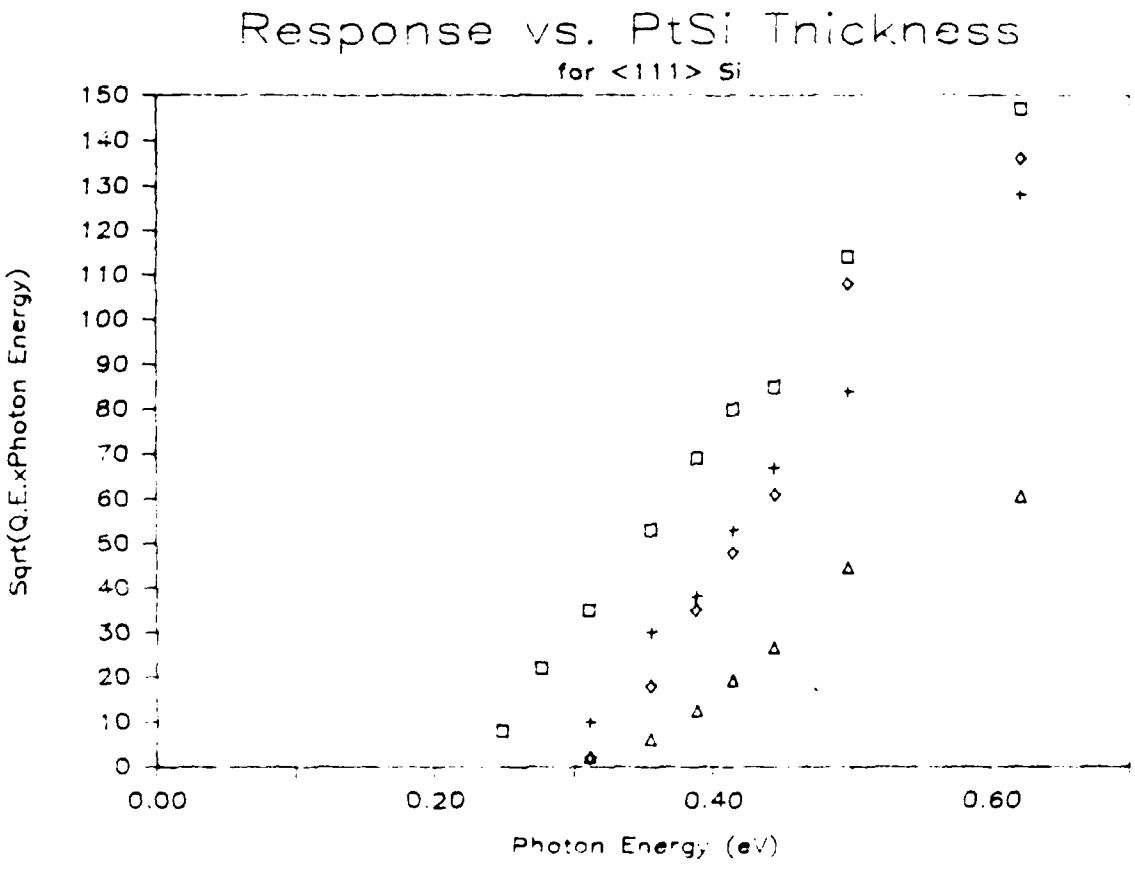
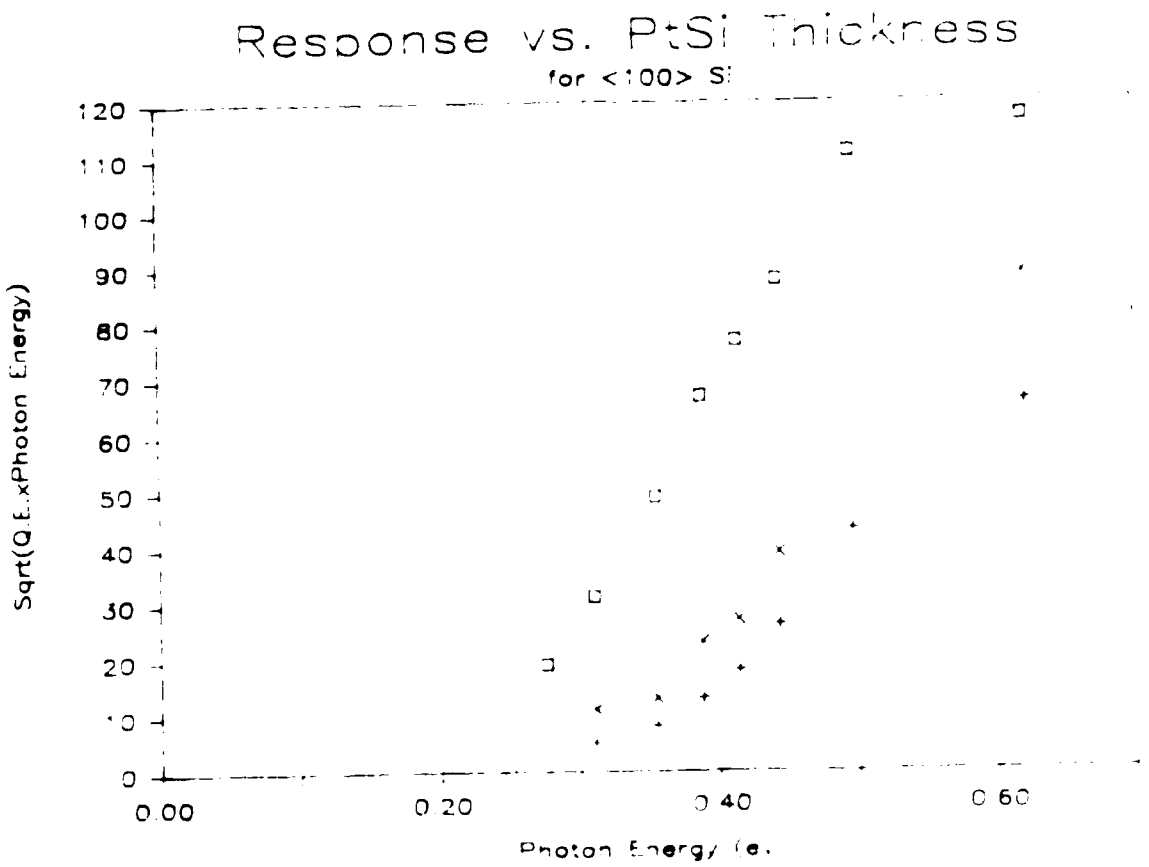


Figure III-29 - Response Vs. PtSi Thickness for (111) Si

(1289M)



X 10A PtSi (1mm) MBE Anneal T = 400°C

□ 40A PtSi (1mm) T = 425°C

• 80A PtSi (1mm) T = 425°C

Figure III-30 Response Vs. PtSi Thickness for (100) Si

(1289H)

evaporators. ATL films thicknesses may be slightly less than stated since this was observed with cross-sectional TEM pictures on earlier films fabricated at ATL. This would account for the response overlap of films with 20A and 40A layers of PtSi.

Also, it is noted that low energy curvature in the Fowler plot disappears as the film thickness decreases. This could be electron phonon effects explained by Mooney and Silverman[8]. Figure III-30 shows a similar result for 40A and 80A PtSi films on (100) Si. The thin 10A MBE film data is presented for completeness but the data is suspect since prior to the Pt deposition, visual inspection of the Si surface showed evidence of pitting, the possible result of a prior, pre-oxide clean. Had the resources not been exhausted, other 10A PtSi films would have been fabricated and tested.

Figure III 31 overlays the 80A and 40A response curves on both substrate orientations and the low energy curvature appears to be independent of substrate orientation Figures III 32 and III 33 graphically show the effect of decreasing the PtSi thickness and the substrate orientation on the Schottky barrier value and the Fowler coefficient However, the extrapolation of the energy barrier values for the thicker film is complicated by the low energy structure The trend is toward increasing C_1 and decreasing Ψ_B as the PtSi thickness decreases with only a slight dependence on the substrate orientation No improvement in response is observed on PtSi diodes formed on (111) Si vs (100) Si for the same film thicknesses

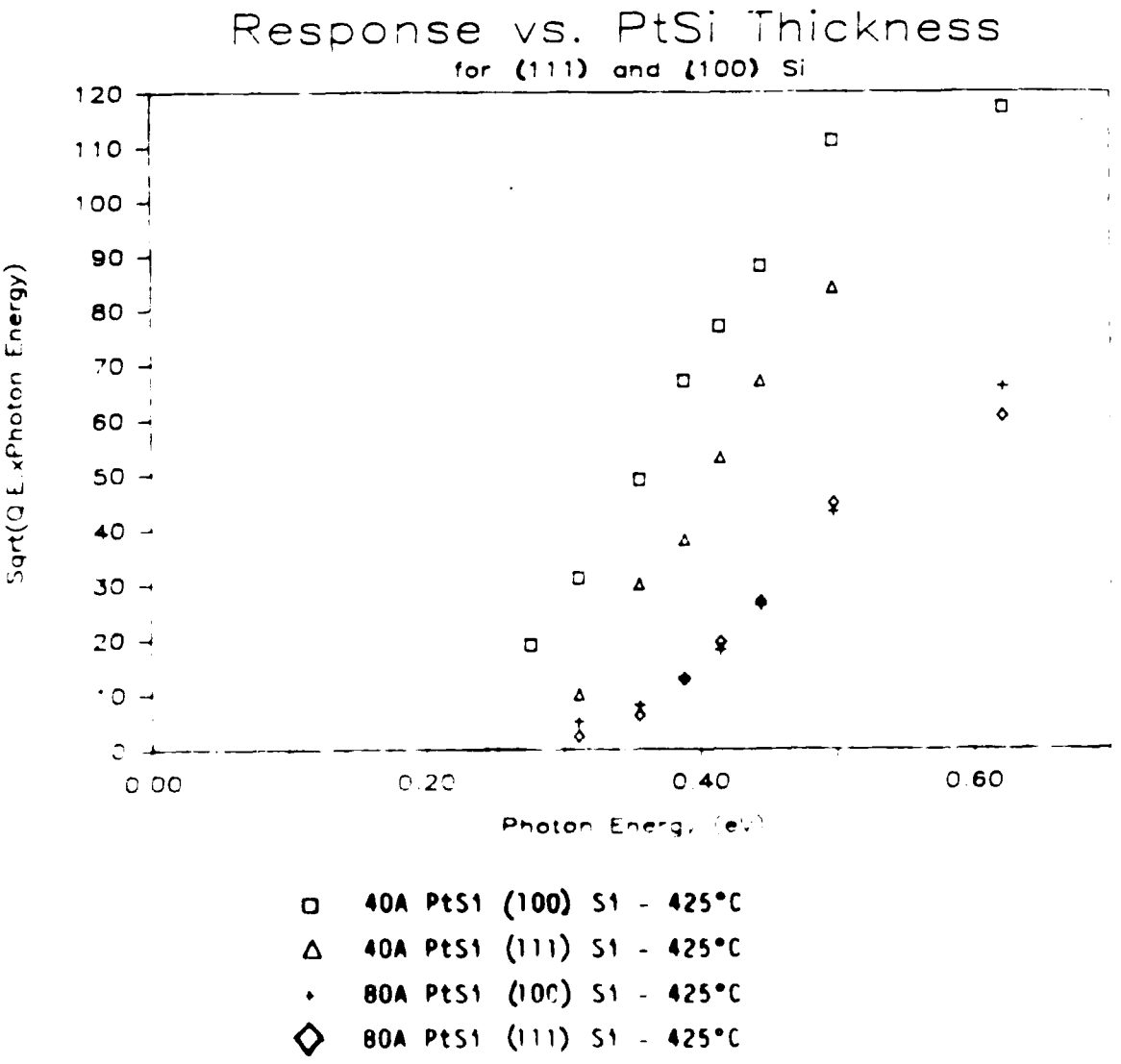


Figure III 31 Overlay of Response Curves for PtSi on (111) and (100) Si

(1289H)

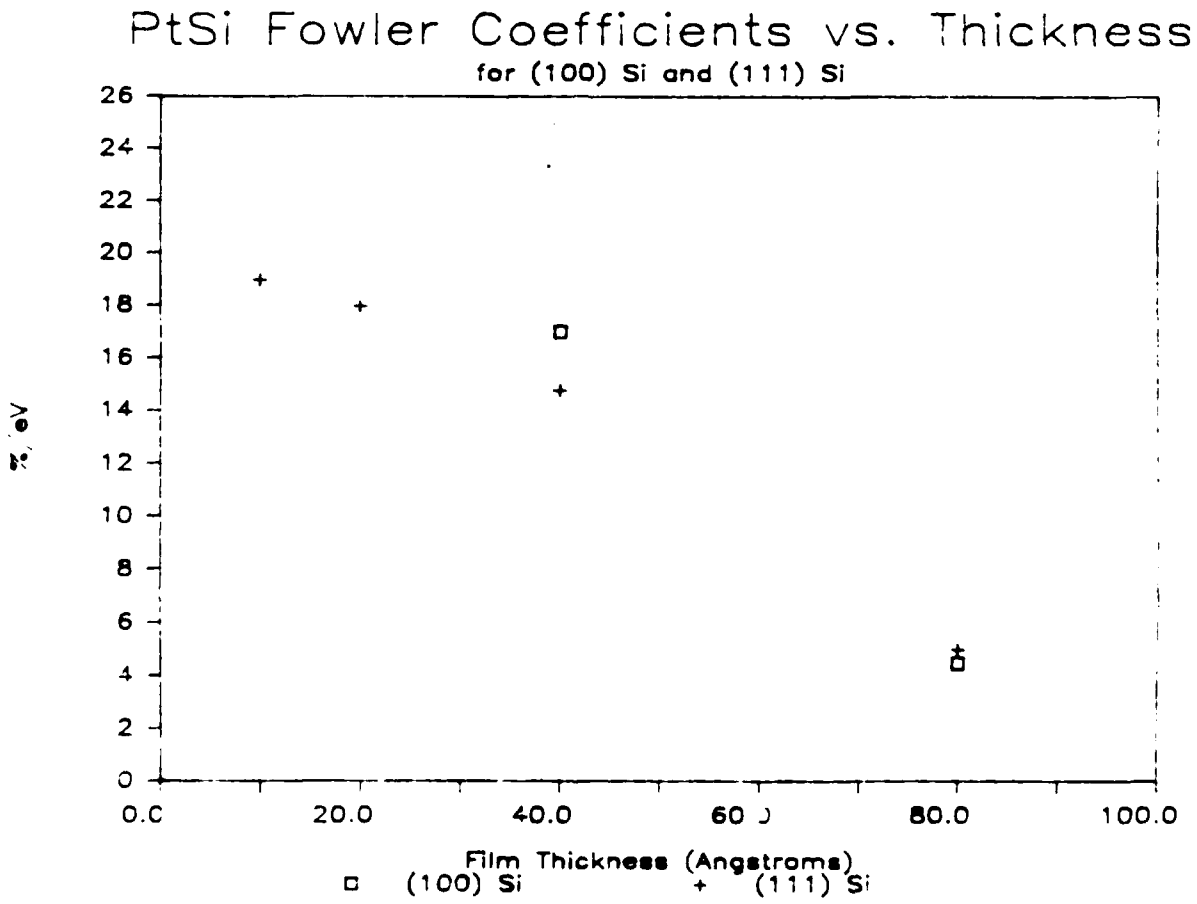


Figure III-32

(1289H)

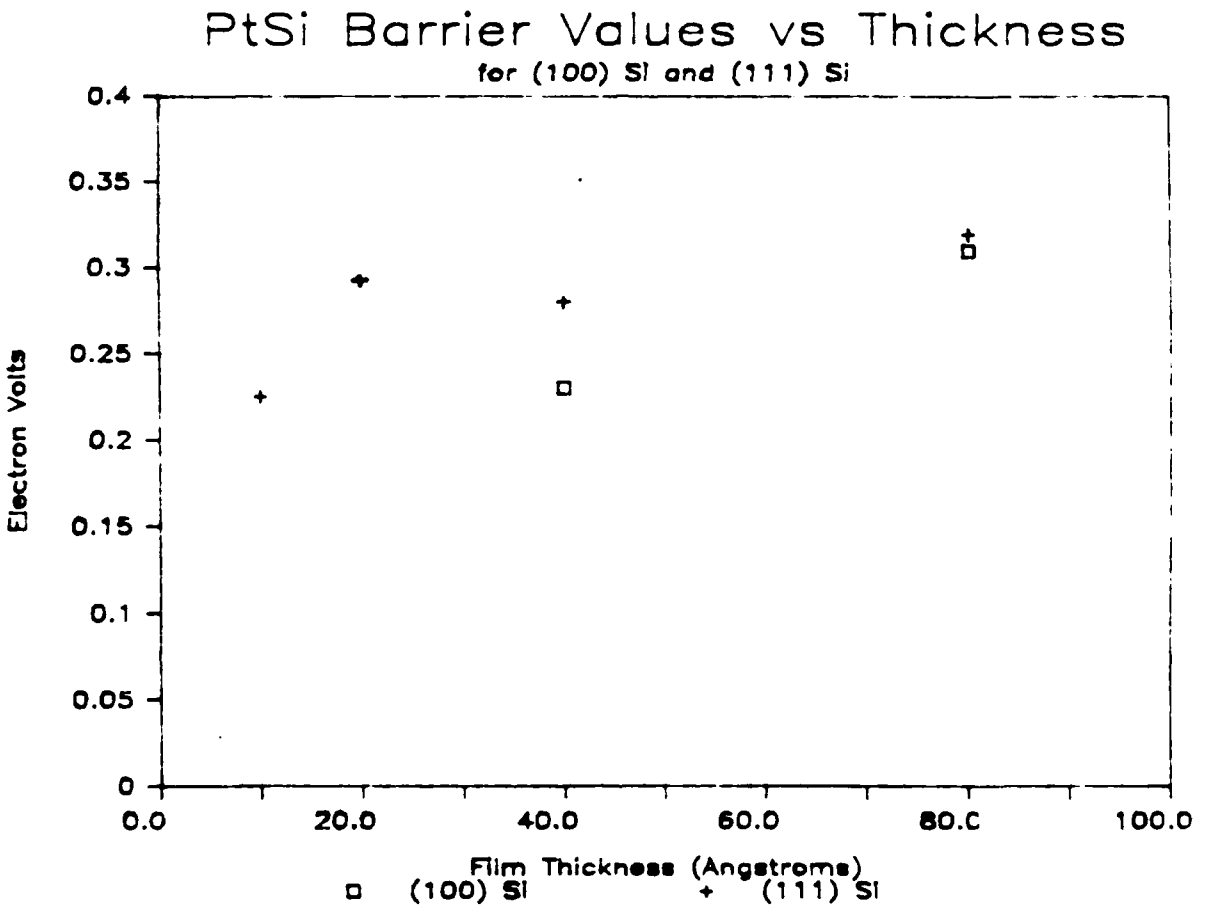
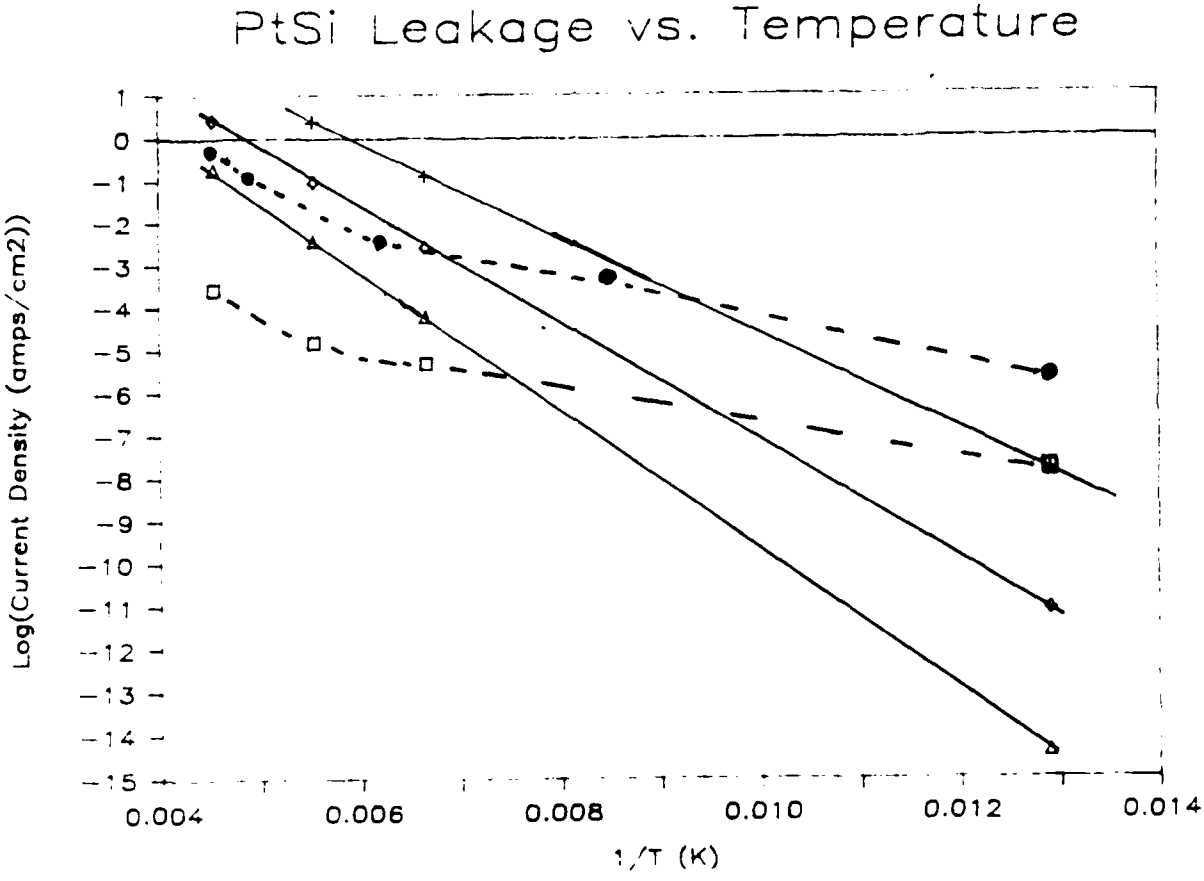


Figure III-33

(1289H)



+ Φ_B = .20eV (theoretical)

◇ Φ_B = .25eV "

△ Φ_B = .30eV "

□ Data from 10A PtSi film on (100) Si (0.5v rev. bias)
MBE - ~400°C anneal

• Data from 20A PtSi film on (111) Si (3 v. rev. biased)
MBE 560°C anneal

Figure III-34

(1289H)

Leakage data and theoretical leakage plots for PtSi Schottky diodes are shown in Figure III-34. The (100) Si substrate data is presented because it is the lowest leakage observed, but was observed on the same diodes (10A PtSi on (100) Si, MBE) which appeared to have the Si surface pitted prior to the Pt deposition.

The data from the 20A PtSi film on (111) Si (reverse biased ~3 volts) is more typical of what was observed. At temperatures between ~160K to ~77K, a slope of ~.1eV was observed which could be attributed to surface state traps. Above ~160K the leakage asymptomatically approaches an electrical barrier value of ~.2eV.

IV. SUMMARY

The Final Report covers the period of January 1984 to April 1986 in a program designed to determine the optimum metallurgy for fabricating PtSi/p-Si Schottky diodes for infrared detection in order to improve their quantum efficiency by a factor of 2 over the state of the art of PtSi Schottky diodes. Results and accomplishments made during this period include:

- Development of a internal photoemission model as a function of film thickness, grain size, degree of epitaxial formation and defect density with main results as follows:
  1. Diffuse photon-electron scattering of the metal/semiconductor interface has significant influence on photoyield depending upon the ratio of the film thickness to the hot electron mean free path d/L^*.
  2. For $d/L^* > .2$, the photoyield is degraded for a rough interface as compared to a smooth interface a change of a factor of ~2 for $d/L^* = 1$.

- Crystallographic characterization of PtSi films formed on (100) and (111) Si including RED, Auger Analysis, Planar and Cross-section TEM leading to the following results.

1. Electron diffraction analysis shows that for both substrate orientations the silicide phase formed was orthorhombic PtSi which is the desired phase of the several possible Pt_xSi_y phases.

2. PtSi on (111) Si is epitaxially related to the Si substrate. The orientation relationship is:

   (010) PtSi parallel to (111) Si for the film and wafer planes;
   [002] PtSi parallel to <220> Si in the plane

   Three equivalent crystallographic variants of this orientation relationship are possible, and the PtSi film is composed of all three variants in apparently equal fractions.

3. PtSi on (111) Si nucleates and grows as islands, however, a continuous film is formed. Impingement of boundaries of similar variants produces a larger interconnected grain structure than that which would be expected for island growth. Furthermore, an analysis of Moire fringe contrast indicate that the impingement boundaries between unlike variants have a high degree of lattice matching and are, therefore, low energy boundaries.

4. 20A PtSi films formed on (111) were continuous and epitaxially related to the (111) Si surface similar to the thicker 80A PtSi film. However, strain evidence appeared on the diffraction patterns implying partial constraint of the PtSi film to a pseudohexagonal cell close to the hexagonal cell of the (111) Si.

5. PtSi on (100) Si produces a near random, fine grain, polycrystalline film. A slight degree of preferred orientation is observed. Oblique views of cross-sectional specimens indicate that the grains of PtSi are thicker at the center than at the boundaries. Nonetheless, a fairly continuous film is produced.

6 No direct observation of the defect structure at the PtSi/Si interface was made. However, the interfacial roughness is less for PtSi/(111) Si than for PtSi/(100) Si. This observation is expected for an epitaxially related film versus a randomly related film. The epitaxial relationship of PtSi/(111) Si would suggest a lower energy interfacial structure than for randomly oriented PtSi (100) Si. Furthermore, the thickness uniformity of PtSi/(111) Si is better than for PtSi/(100) Si.

- [illegible] response and leakage measurements were made on the fabricated PtSi [illegible] formed with different PtSi thicknesses, substrate orientation [illegible] and [illegible], anneal temperature and evaporation systems.

1. No improvement in the response data was observed by varying the substrate orientation from (100) Si to (111) Si for a PtSi film of the same thicknesses. This result coupled with the photoyield data implies a d/L* ratio $\leq$ .2 or an L* > 500A.

2. The best C_1 value was ~ 19%/eV and Φ_B = .225eV obtained on an MBE ~ 10A PtSi formed on (111) Si. C_1's varied from 5%/eV to 19%/eV and Φ_B from ~32eV to .225eV as the PtSi thickness varied from 80A to 10A. Similar results were seen with films on the (100) Si.

3. Curvature on the low energy end of Fowler plots was observed for diodes having an ~80A film thickness regardless of the substrate orientation. This curvature disappears as the film thickness decreases and is thought to be due to electron phonon scattering effects of low energy photo-electrons.

- Reverse biased diodes exhibited excess leakage at temperatures below ~160K. Above 160K, the leakage approached theoretical leakage with a barrier of ~.2eV. The slope of the L_n (current density) vs. 1/T curves, exhibited below 160K, showed a linear relationship with a barrier of ~.1eV. This excess leakage could be due to a surface trap from a source such as the AP Silox deposited after the silicide. The problem has been resolved by the people at RADC, Hanscom AFB and is not inherent in a PtSi diode.

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(1289H)

V. Appendix

Diode Response Data on <111> Si

(Figure III-28)

10A PtSi(0.2mm)

$\sqrt{QE \times h\nu} \times 10^{-3}$

hν(eV)	Diode 1	2	3	4
.621	159	154	188	192
.497	128	135	147	150
.444	99	102	109	102
.414	92	92	96	88
.388	77	77	82	77
.355	63	63	63	61
.311	40	40	41	38
.276	22	24	24	19
.248		too noisy		

10A PtSi(1.0mm)

$\sqrt{QE \times h\nu} \times 10^{-3}$

hν(eV)	Diode 1	2	3	4
.621	142	124	159	159
.497	109	95	129	120
.444	82	78	93	87
.414	79	74	86	81
.388	68	61	75	69
.355	54	49	58	53
.311	35	32	39	34
.276	23	21	24	22
.248	13	0	too noisy	

20A PtSi(0.2mm)

$\sqrt{QE \times h\nu} \times 10^{-3}$

hν(eV)	Diode 1	2
.621	205	205
.497	169	164
.444	107	88
.414	84	65
.388	65	52
.355	42	28
.311	15	0

20A PtSi(1.0mm)

$\sqrt{QE \times h\nu} \times 10^{-3}$

hν(eV)	Diode 1	2	3
.621	133	133	142
.497	105	105	114
.444	61	59	63
.414	48	47	49
.388	35	34	35
.355	18	18	19
.311	3	3	0

Table A-1

(1417H)

Diode Response Data on <111> Si

(Figure III-29)

10A PtSi

$\sqrt{QE \times hv} \times 10^{-3}$

hv(eV)	Diode 1	2	3	4
.621	142	124	159	159
.497	109	95	129	120
.444	82	78	93	87
.414	79	74	86	81
.388	68	61	75	69
.355	54	49	58	53
.311	35	32	39	34
.276	23	21	24	22
.248	13	0	too noisy	

20A PtSi

$\sqrt{QE \times hv} \times 10^{-3}$

hv(eV)	Diode 1	2	3
.621	133	133	142
.497	105	105	114
.444	61	59	63
.414	48	47	49
.388	35	34	35
.355	18	18	19
.311	3	3	0

40A PtSi

$\sqrt{QE \times hv} \times 10^{-3}$

hv(eV)	Diode 1	2	3
.621	130	126	128
.497	86	83	82
.444	70	68	63
.414	56	53	51
.388	39	39	36
.355	31	32	28
.311	10	10	10
.248	4	4	4

80A PtSi

$\sqrt{QE \times hv} \times 10^{-3}$

hv(eV)	Diode 1	2
.621	56	60
.497	41	46
.444	24	26
.414	18	18
.388	11	13
.355	6	6
.311	2	1

Table A-2

Diode Response Data on <111> Si

(Figure III 30)

10A PtSi

$\sqrt{QE \times hv} \times 10^{-3}$

hv(eV)	Diode 1	2
.621	91	92
.497	71	71
.444	40	40
.414	38	38
.388	25	25
.355	15	15
.311	13	12
.276	too noisy	

20A PtSi

$\sqrt{QE \times hv} \times 10^{-3}$

hv(eV)	Diode 1	2	3	4
.621	118	126	114	112
.497	113	116	106	106
.444	88	92	93	80
.414	78	82	74	72
.388	71	72	64	63
.355	50	53	46	45
.311	32	33	30	29
.276	22	18	19	18
.248	too noisy		9	9

80A PtSi

$\sqrt{QE \times hv} \times 10^{-3}$

hv(eV)	Diode 1	2	3	4
.621	57	57	73	77
.497	42	51	40	37
.444	24	33	24	21
.414	17	22	16	14
.388	7	10	10	6
.355	4	6	4	4

Table A-3

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